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ANUAL # VOL 1 of 2

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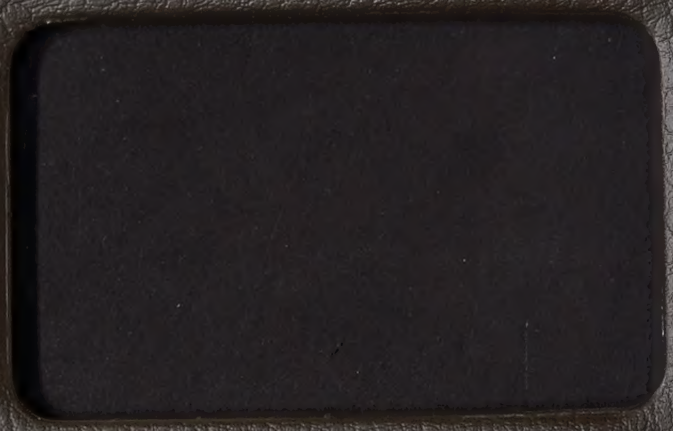
TECHNICAL DATA



1170
FREQUENCY RESPONSE ANALYSER

(Includes 1172-M1)

Volume 1

MP MASTER
MA20020
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MANUAL # VOL 1 of 2

REVISIONS				
SYM	DESCRIPTION	EFFECTIVITY	DATE	APPROVED

31589

INSTRUCTION MANUAL ADDENDUM

		DRAWN BY	DATE 1/16/75	EMR / EMR Schlumberger — EMR TELEMETRY, WESTON INSTRUMENTS, INC., BOX 3041-SARASOTA, FLORIDA 33578
		DESIGNER	1-17-75	
		CHECKER	1/19/75	MODIFICATION DRAWING FREQ RESPONSE ANALYZER MODEL 1172-M1
		DESIGN ENGINEER	1-17-75	
Final	C4658	PROJECT ENGINEER	1-19-75	SIZE A | CODE IDENT NO. 06141 | DRAWING NO. 31589 | REV
NEXT ASSY NO.	USED ON	APPROVED		
APPLICATION				
III	II	APPROVED		SCALE — | SHEET 1 OF 4
GRADE	CATEGORY			

GENERAL:

This document describes the requirements to convert a Solartron standard Model 1172 Freq Response Analyzer to a Model 1172-M1.

PURPOSE:

The purpose of the -M1 is to convert a standard 1172 for 10 ohm generator output impedance and 50 to 400 Hz operation.

MODIFICATIONS:

The following steps are required to perform the modification:

1. On mother board A1729001, remove resistor R2 (190 ohms) and replace with jumper wire for 10 ohm output impedance.

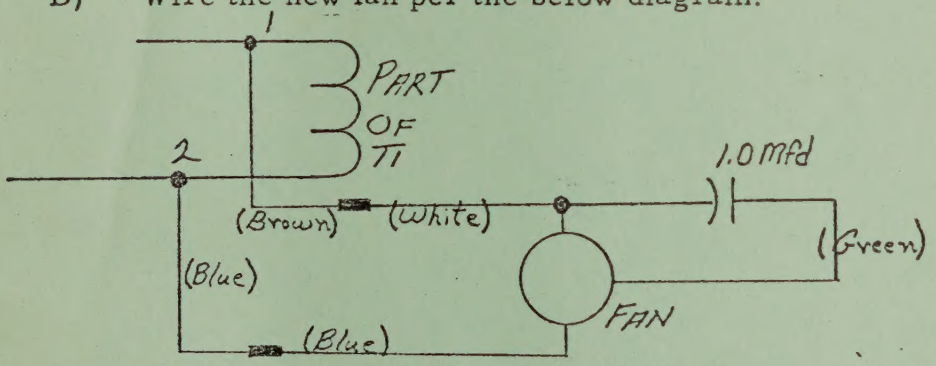
2. As shown on sheet 4 of this modification, for 50 to 400 Hz operation:

   A) Remove existing cooling fan and replace with Item #4.

   B) Replace the two 6-32 hex nuts holding the bracket assy (Item #5) to the fan with Item #1.

   C) Using Item #3 sleeve the leads of Item #2 and then solder in place.

   D) Wire the new fan per the below diagram.



3. Mark Equipment Nameplate No. 31538 (Stock No. 196-99-00295) with Assy No. 31589 and Model No. 1172-M1 per EMR 13406.

EDC

SIZE	CODE IDENT NO.	DRAWING NO.	
A	06141	31589	
SCALE -/-		SHEET	2

TEST:

1. 10 ohm output impedance

   A) Program 1172 for 1.000V and 100 Hz generator output.

   B) Terminate generator output with a 10 ohm, 1%, 1/8W resistor to ground. Verify generator output voltage is $\geqq$ 0.5V rms.

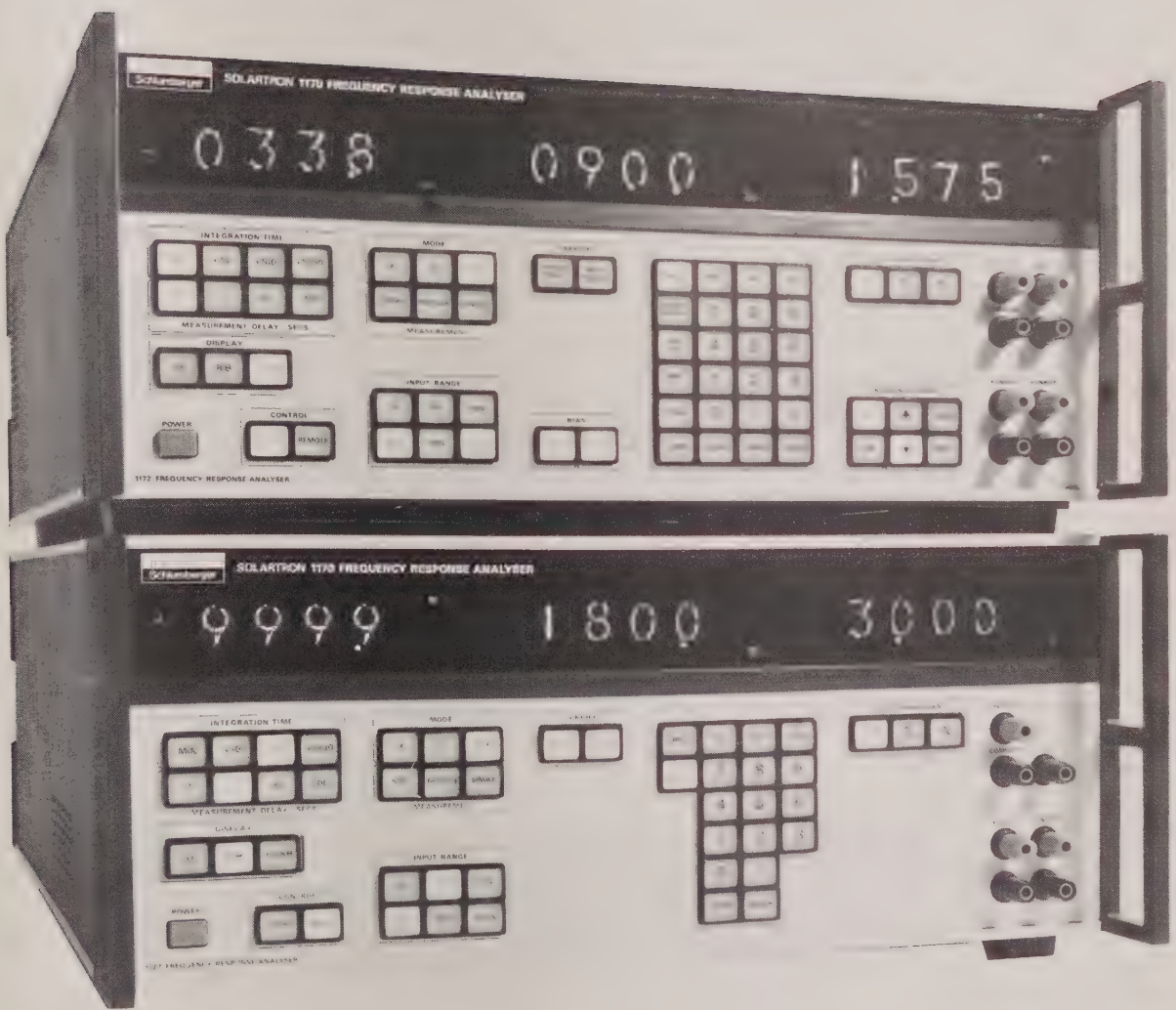
2. 50 Hz to 400 Hz operation:

   A) Perform a cursory check utilizing both the generator and correlator portions of the 1172 at 50 Hz and 400 Hz.

EDC

SIZE	CODE IDENT NO.	DRAWING NO.	
A	06141	31589	
SCALE			SHEET 3

1170 FREQUENCY RESPONSE ANALYSER



Part No: A1720200

Date of Issue : September 1974

Schlumberger

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SERVICING MANUAL

19 ©74

Printed in England by The Solartron Electronic Group Ltd

Introduction to the Servicing Manual

As the 1170 Series Frequency Response Analyser requires virtually no routine servicing, this manual is primarily intended to assist the Service Technician in the task of fault diagnosis and rectification.

Module Identification

An instrument is identified by the type number of its Generator Assembly, which is a plug-in module to the 1170 Analyser.

It will be noted that this Servicing Manual makes little reference to the Type 1177. Users of this type of instrument should note that the boards and assemblies used in the 1177 are identical to those of the 1172 and are therefore identified as such.

The Mainframe of the 1170 Analyser is common to all models.

Arrangement of the Manual

The manual is divided into three main sections as follows:-

1. **The Functional Description**

   This section includes the technical description, the circuit diagrams and the use of special diagnostic equipment for fault finding.

2. **The Physical Desciption**

   This section includes a description of the assembly of the instrument, parts lists and component layout diagrams for the pcb's and a list of all the common connections throughout the instrument.

3. **Calibration Procedure**

   Includes testing and setting-up methods for the pcb's and complete assemblies.

A separate manual contains the equivalent information for the peripheral units which occupy positions 18 to 22 of the 1170.

The relationship between the circuit diagrams and the printed circuit boards is shown in the 1170 Circuit Diagram Allocation Chart which is produced in both Section 1 and Section 2.

This chart also defines the functional areas of the instrument.

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	Circuit Diagrams	
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	(not yet issued)	

Date of Issue : October 1974

SECTION 1 Functional Description

Introduction

This section is divided into three sub-sections, namely:-

1.2 Technical description

1.3 The circuit diagrams

1.4 Fault Finding methods

The technical description in Section 1.2 is provisional and will be later re-issued in an expanded form.

Section 1.4 is not included in this printing as it is based upon the use of special diagnostic test equipment not yet fully developed.

Your Schlumberger agent will keep you informed as to the availability of these sections.

1.2 Technical Description

The description which follows is a provisional issue. For this reason is will be found that some parts of the instrument are not described. It is also the reason for the unusual page numbering system used. As this is an extract from another publication the pages are numbered 141 to 183.

INTRODUCTION TO MACHINE ORGANISATION

Note: For 1177 readers, ignore any references to SWEEP or BIAS.

The 1170 is divided into two parts - the "Generator" section and the "Analyser" (correlator) section.

The Generator section produces an electrical sine wave output signal. The amplitude and frequency of this signal are controlled from the keyboard.

The Analyser accepts an electrical input signal, and, when commanded from the keyboard, makes a measurement on this signal and displays the results.

Measurements may be made on either of two input channels (channel X or Y), and the most recently measured results on either channel (X or Y), or the ratio between them (i.e. "point to point" result, Y/X) may be displayed. The results may be displayed in any of three co-ordinate systems (A and jB, R and θ, or log R and θ).

The instrument contains a data store (MOS STORE), in which are stored all the results, as well as the generator operating parameters, the frequency sweep parameters and the bias generator output voltage. It also contains an "arithmetic unit", which is used to calculate the results, and a "control logic" section, which controls the overall sequence of operations performed by the machine.

The generator parameters, frequency sweep parameters and bias voltage may be altered from the keyboard when the instrument is not measuring. Some action by the control logic and arithmetic unit is necessary when changing the generator parameters - the frequency sweep parameters and bias voltage may be changed directly via the keyboard. Any one of these parameters may be displayed in the "Keyboard Display", by touching the appropriate key.

The "Results Display" can display any one set of results from the store in accordance with the setting of the A, B; R, θ; log R, θ and X; Y; Y/X keys.

MEASUREMENT SEQUENCES

The simplest measurement which the machine can make is made with the following front panel touch key settings:

Sweep OFF

SINGLE Measurement

Channel X

Reject Bias OFF

Fixed input voltage range

To make a measurement under these conditions, the input is first analysed by the "*correlation*" process (see CORRELATION IN THE 1170). This gives an intermediate result, which, after division by "integration time", T (by the arithmetic unit), provides results in A, jB form which are placed in the MOS store. Further calculation by the arithmetic unit gives the single channel results in the other co-ordinate systems, which are also stored. The "point to point" results are then calculated and stored, using the previously measured results for channel Y from the store.

The other functions which can be provided by the instrument, when requested from the touch keys, are accomplished as follows:

1. **Autorange**	Measurement starts on the 10mV range. If the instrument overloads, the measurement is terminated immediately, the input range is increased by a factor of 10, and a new measurement commenced. This is repeated, if necessary, until the 100V range is reached.
2. **Reject Bias.**	A measurement is made in the "Measure bias" mode. The single channel calculation proceeds to the point where the in-phase component (real part) is known. A voltage of this magnitude is then generated internally and applied as a "backing-off" voltage to oppose the bias, and a new measurement taken.
3. **Point to point.**	A set of relays ("input relays") is provided so that the input of the analyser can be connected either to the channel "X" terminals or to the channel "Y" terminals. A channel "X" measurement is taken and the single channel results calculated and stored. The input relays are then changed to channel "Y", and another measurement taken, and single channel and point to point results calculated and stored.
4. **Frequency sweep.**	Before the measurement, a new frequency is calculated by the arithmetic unit, using the parameters which have been entered into the store from the keyboard (f MIN, f MAX, Δ f LOG, Δ f LIN). The generator frequency is changed to this new frequency. A delay depending on the setting on the "measure delay" touch keys is then allowed to elapse before commencing the measurement. This allows any transient in the "system on test", due to the change in frequency, to die away.
5. **Recycle**	A continuous series of measurements is initiated. Between each measurement, a delay is allowed to elapse depending on the setting of the "measure delay" touch keys.

INTRODUCTION TO THE GENERATOR

The Generator section of the instrument generates a sine, square or triangular waveform stimulating signal which is used to excite the system under test.

Clock Generator

This section of circuitry consists essentially of a synthesizer employing an R.F. varactor - tuned oscillator and a first order programmable phase-locked loop. The output is a clock frequency of 2000f (200f on the 10kHz range) where f is the required output frequency.

The clock is utilised by the generator to produce the sine wave output, and also by the arithmetic system to produce the sine and cosine signals required for correlation. A number of crystal controlled fixed frequencies are also produced for use throughout the system, e.g., 10MHz, 1MHz, 500kHz, 200kHz and 100kHz.

Waveform Generator

An up/down counter and D.A.C. produce an analogue ramp which is converted by means of a seven section shaping network into a low-distortion sine wave of fixed amplitude. Provision is made to produce ramps or square waves by changes of operation. Only one output waveform shape can be produced at any one time.

Bias and Output Volts Control

This converts two pulse sequences, derived from the store data for output volts and bias, into two dc levels, using a precision integrator and two sample/hold circuits.

Programmable Attenuator

This is effectively a multiplier, one input being the fixed amplitude signal from the waveform generator, the other being the dc level proportional to the required output voltage from the bias and output volts control.

Output Amplifiers

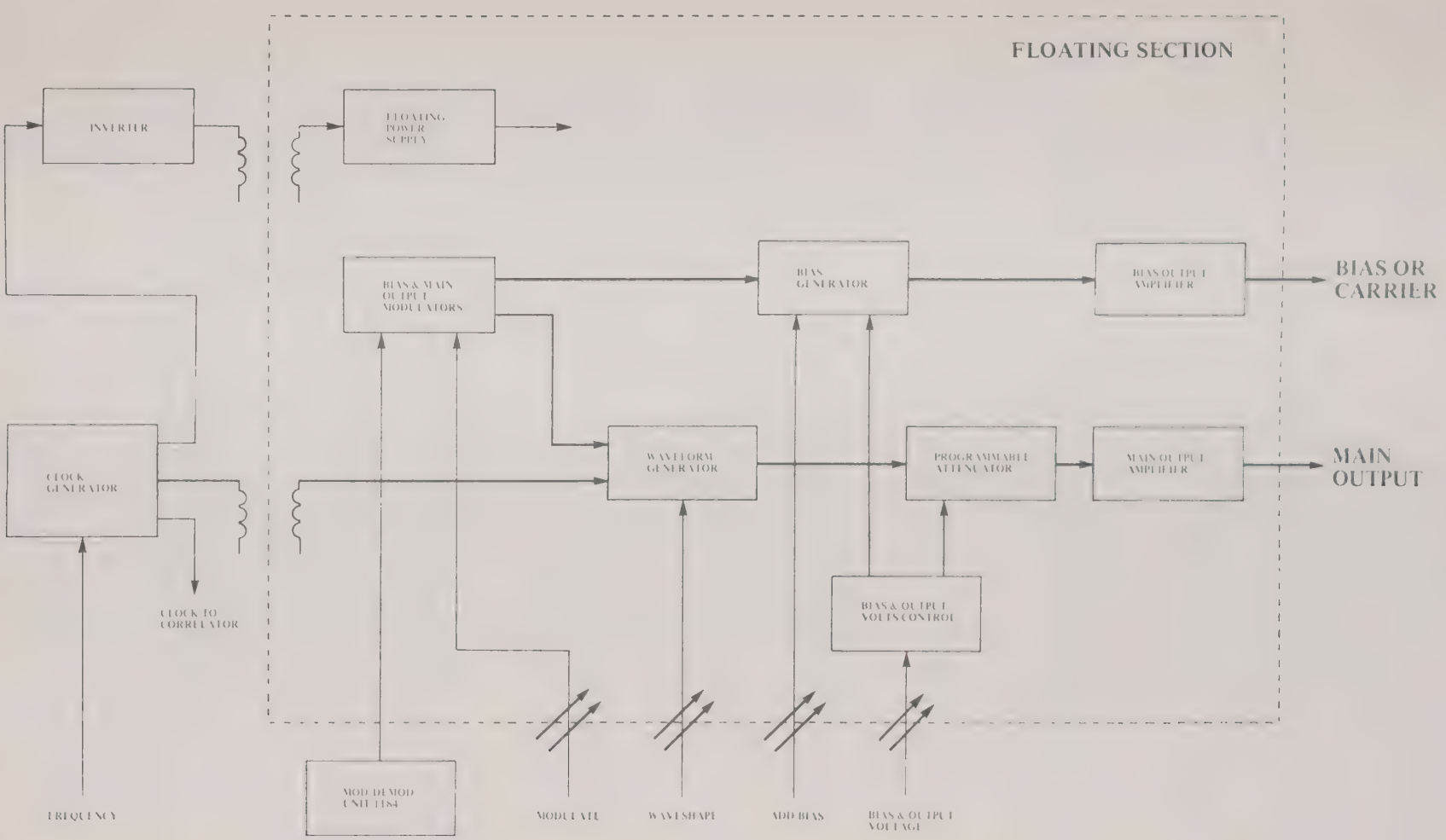
These produce the necessary voltage and power to drive the system under test (up to 40V p.p in ac carrier mode, and up to 100mA load current).

Modulators

When systems employing ac carrier modulated signals are measured, the output signals have to be multiplied by a sine wave (carrier reference). The 1184 Mod/Demod Unit converts this reference sine wave into a binary signal with mark/space modulation, and two mark/space multipliers are used in the generator to produce modulated outputs.

Power Supplies

The 100kHz clock output from the clock generator drives an inverter which, via a transformer and bridge rectifiers, produces all the voltage levels to operate the generator.



BLOCK DIAGRAM - 1172 GENERATOR

CORRELATION IN THE 1170

INTRODUCTION

The 1170 is a "**Frequency Response Analyser**". It is usually used to measure the response of a system to a sine wave stimulating signal over a range of frequencies. Normally the stimulating signal is the output of the 1170 generator, a sine wave at frequency f.

The output of the system on test, can be split, by means of Fourier analysis, into a fundamental response (a sine wave at frequency f), harmonics (sine waves at integral multiples of frequency f) due to the non-linearities in the system on test together with any non-harmonically related noise. The 1170 measures the *fundamental* sine wave response, ignoring as far as possible any harmonics or random noise present. It is resolved into two components - one due to a sine wave IN-PHASE with the generator output, and one due to a sine wave in QUADRATURE with the generator output. This enables the PHASE response of the system to be measured, as well, as the AMPLITUDE response.

Measurements made over a range of frequencies enable the system frequency response, in phase and amplitude, to be built up.

BASIC PRINCIPLES

The 1170 uses a correlation process to measure the in-phase and quadrature components of the fundamental response of the system.

The generator output is a signal of the form $v_G = A_G \sin 2\pi ft$.

The output of the system on test is a signal $v_c(t)$..

To calculate the in-phase component at frequency f, this signal is multiplied by a signal $\sin 2\pi ft$, and integrated with respect to time, for a whole number of cycles N. This gives the result:

$$I_A = \int_0^T v_c\ (t)\ \sin 2\pi ft\ dt \qquad \text{where } T = \frac{N}{f}$$

Similarly the quadrature component is calculated by forming the integral,

$$I_B = \int_0^T v_c\ (t)\ \cos 2\pi ft\ dt$$

If the components of $v_c\ (t)$ are A $\sin 2\pi ft$ (in-phase) and B $\cos 2\pi ft$ (quadrature) respectively, then:

$$I_A = \int_0^T (A \sin^2 2\pi ft + B \sin 2\pi ft \cos 2\pi ft)\ dt$$

$$= \tfrac{1}{2}A \int_0^T (1-\cos 4\pi ft)\ dt \quad + \tfrac{1}{2}B \int_0^T (\sin 4\pi ft)\ dt$$

$$= \tfrac{1}{2}AT - \tfrac{1}{2}A \int_0^T \cos 4\pi ft\ dt \quad + \tfrac{1}{2}B \int_0^T \sin 4\pi ft\ dt$$

For a whole number of cycles, the integrals in this expression are both zero, hence:

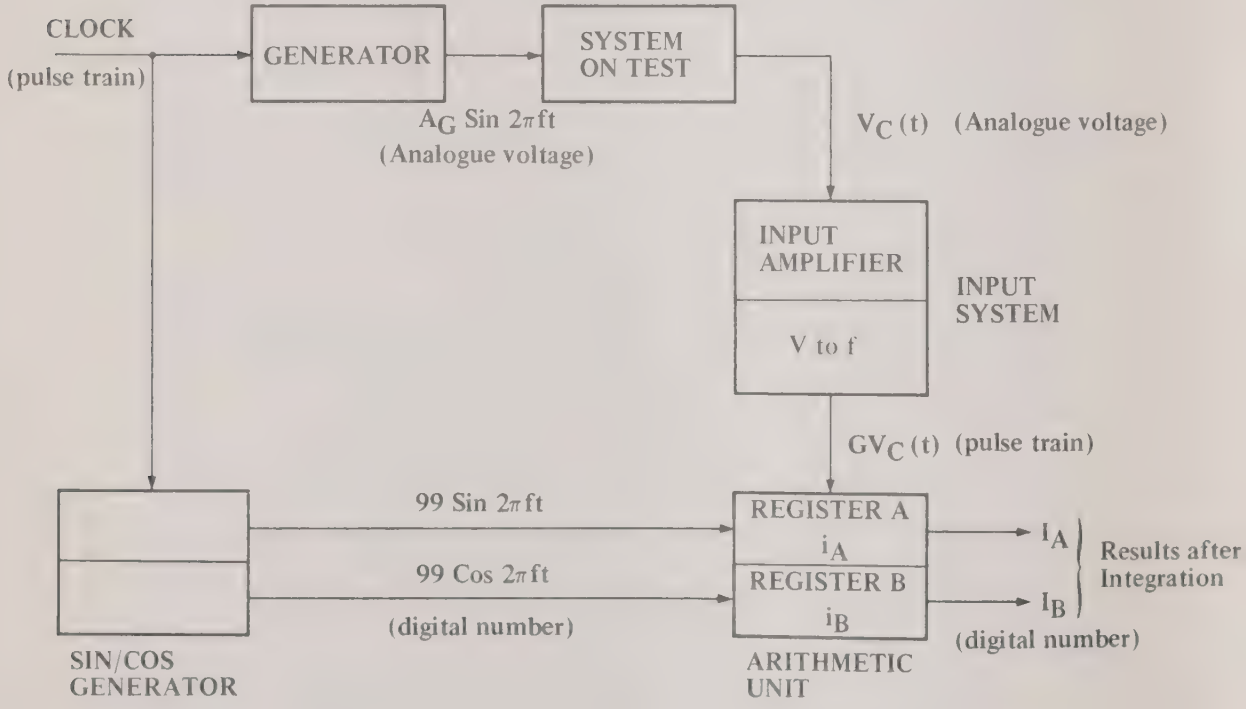
$I_A = \frac{1}{2}AT$. Similarly, $I_B = \frac{1}{2}BT$

Division by time of integration, T, allows the amplitudes of the in-phase and quadrature components, A and B, to be determined.

It can be shown that this method rejects harmonic components of $v_c(t)$ completely, and gives good rejection of random noise, which can be further improved by lengthening the integration time, T.

THE MECHANISM OF CORRELATION

The correlator contains a "sin/cos generator" (board 3), which produces the values of sin $2\pi ft$ and cos $2\pi ft$ necessary for the correlation process. The outputs of the sin/cos generator are two signed 2 digit BCD numbers, each in the range +99 to -99, equal to 99 sin $2\pi ft$ and 99 cos $2\pi ft$. The "sine" value is fed to arithmetic register A (board 5) and the "cosine" value to register B (board 6). These numbers are always available to the arithmetic unit, and follow the generator output sinewave.



CORRELATION IN THE 1170

The output of the system on test, $v_c(t)$ is applied to the correlator input terminals. It then enters the input system (boards 23 & 24), which consists of an input amplifier and a voltage to frequency converter (V to f), with an overall system gain of G pulses per second per volt.

The output of the V to f ($Gv_c(t)$ pulses per sec.) is fed to the arithmetic unit (board 4). On receiving each V to f pulse from the input system, the arithmetic unit adds the current value of "sine", presented to it by the sin/cos generator, to the contents of register A. Likewise, the current value of "cosine" is added to the contents of register B.

If the instantaneous contents of register A are i_A, and of register B are i_B, the rates of increase of the contents of the register are given by:

$$\frac{di_A}{dt} = Gv_c\,(t)\,.99 \sin 2\pi ft \qquad \text{and} \qquad \frac{di_B}{dt} = Gv_c\,(t)\,.99 \cos 2\pi ft$$

The final contents of the registers after the integration process are given by

$$I_A = \int_0^T Gv_c\,(t)\,.99 \sin 2\pi ft\,dt \qquad I_B = \int_0^T Gv_c\,(t)\,.99 \cos 2\pi ft\,dt$$

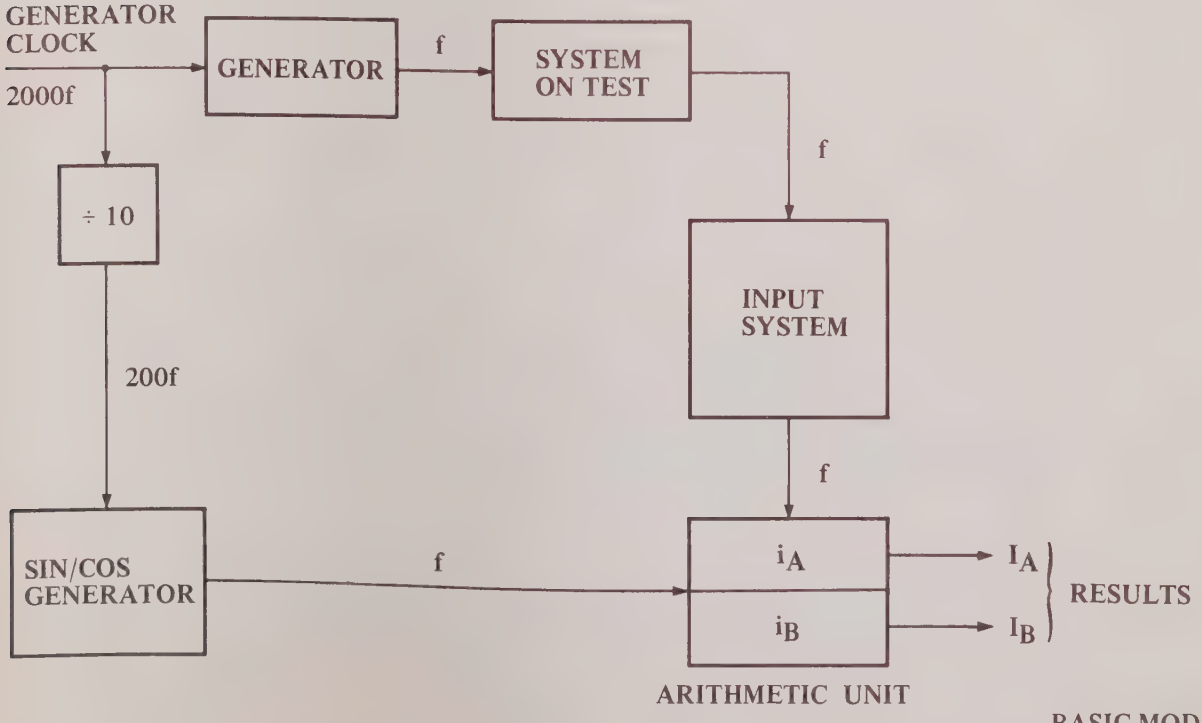
These results, with a suitable scaling factor, allow the in-phase and quadrature components of the system fundamental response to be calculated (see the explanation of the correlation process, above).

MODES OF OPERATION OF THE CORRELATOR

The sin/cos generator input to the arithmetic unit represents a sine wave at a certain frequency (the "correlator frequency"). The V to f signal is derived from the signal present on the analyser input terminals. The characteristics of the correlation process ensure that only the component of this V to f signal which is at the correlator frequency contributes to the result. If the correlator frequency is different from the frequency of the component of the input signal which is to be measured (the "measuring frequency"), the input system must change the frequency of the input signal before it reaches the V to f, so that the desired component will be correlated.

(a) Basic Mode

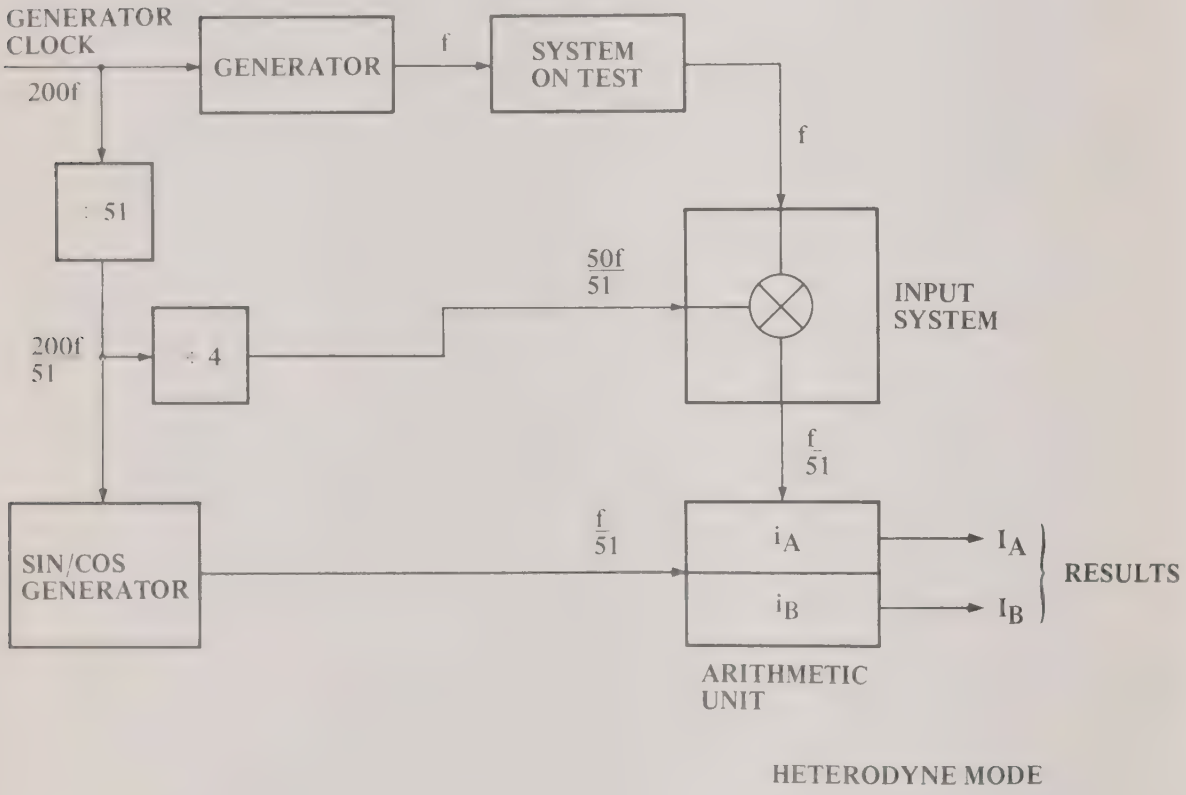
The basic mode of the correlator is used for measuring frequencies below 1kHz. In this mode, the correlator and the generator operate at the same frequency f. The frequency of the generator output sine wave is determined by the frequency of a clock signal (the "generator clock") which contains 2000 pulses for each cycle of output sine wave. The generator clock is thus at a frequency 2000f. This is divided by ten to produce the clock (200f) for the sin/cos generator, which always requires 200 pulses for each cycle. The sin/cos generator output thus represents a signal at frequency f, locked to the generator. The input system does not alter the frequency of the input signal, so the component at frequency f is measured.



BASIC MODE

(b) Heterodyne Mode

The correlator is capable of giving accurate results only up to a frequency of 1kHz. At measuring frequencies from 1kHz to 9.999kHz, the correlator operates at a lower frequency, enabling accuracy to be maintained. On this frequency range, the generator only requires 200 pulses per cycle. The generator clock is at frequency 200f. It is divided by 51 to produce the clock for the sin/cos generator (200f/51). The sin/cos clock is also divided by 4 to give a heterodyning signal at frequency 50f/51. The input system multiplies the input signal by this heterodyning signal, to produce a difference signal at the correlator frequency, f-50f/51=f/51.



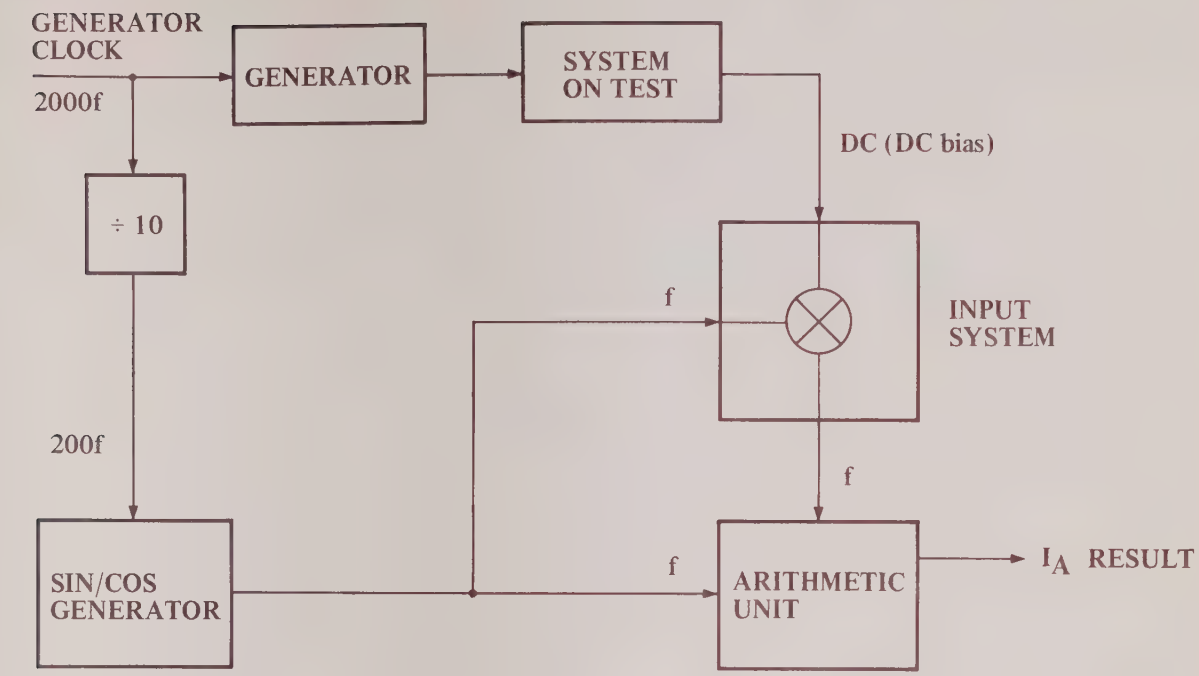
HETERODYNE MODE

(c) Measure Bias Mode

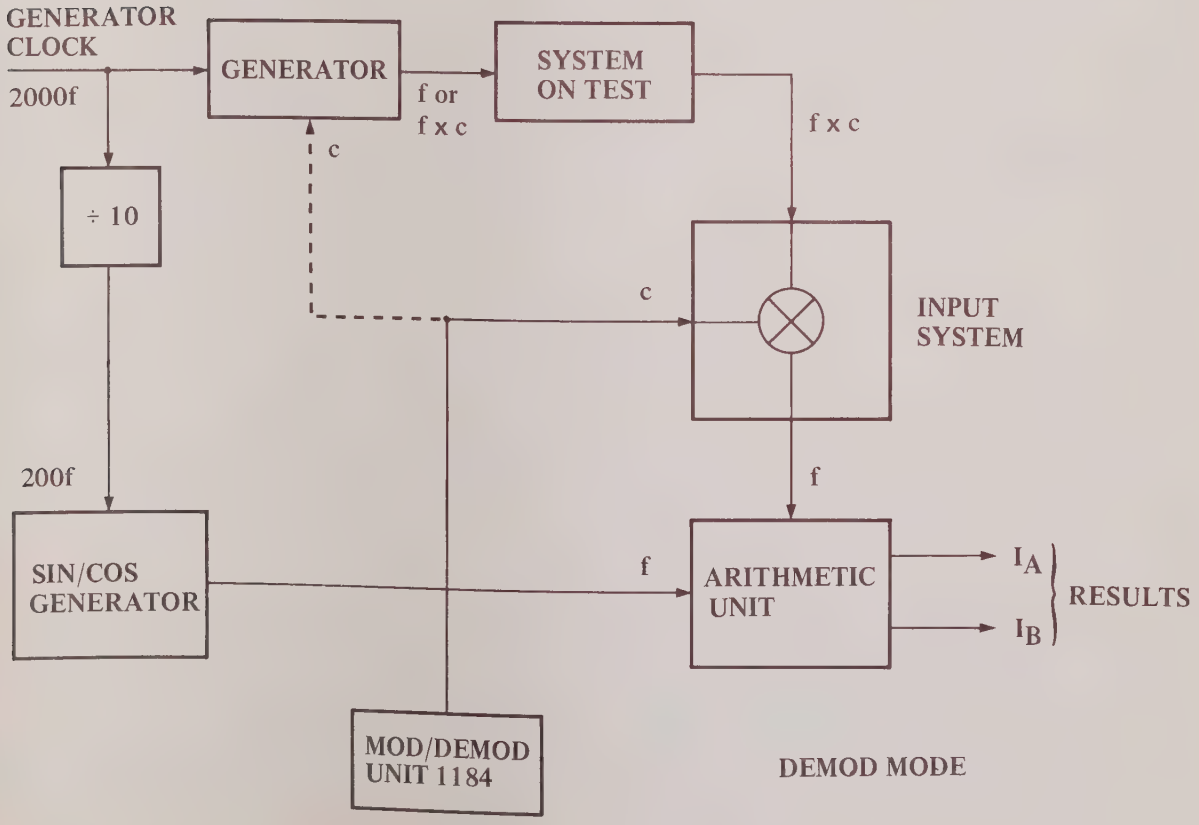
When "Reject Bias" is programmed, the correlator is used to measure the DC voltage on the input terminals, so that a "backing-off" voltage can be generated. This measurement is made in the "Measure bias" mode. The input to the correlator is multiplied by a square wave at the correlator frequency f. This converts any DC present to AC at frequency f, which is then correlated. (The "signal" present at the input terminal in converted to a mixture of DC and harmonics, all of which are rejected by the correlator, and thus does not interfere with the bias measurement).

(d) Demod Mode

When "Demod" is programmed, the output from the system under test is demodulated by multiplying it by a square wave at the carrier frequency c.



MEASURE BIAS MODE



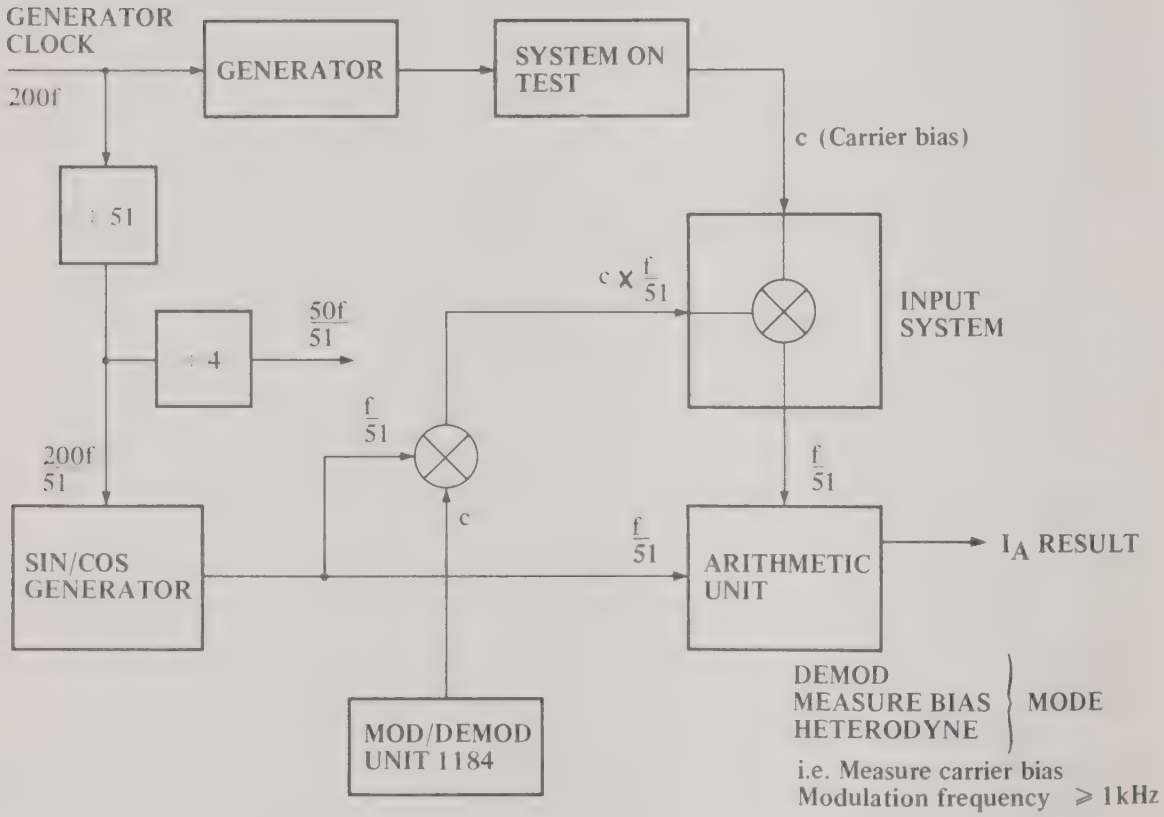
DEMOD MODE

(e) Combinations of modes

All combinations of modes are possible, viz

Measure bias	.	Demod	i.e. measure carrier bias
*Measure bias	.	Heterodyne	
Demod	.	Heterodyne	i.e modulation freq≥1kHz
*Demod	.	Heterodyne	. Measure bias

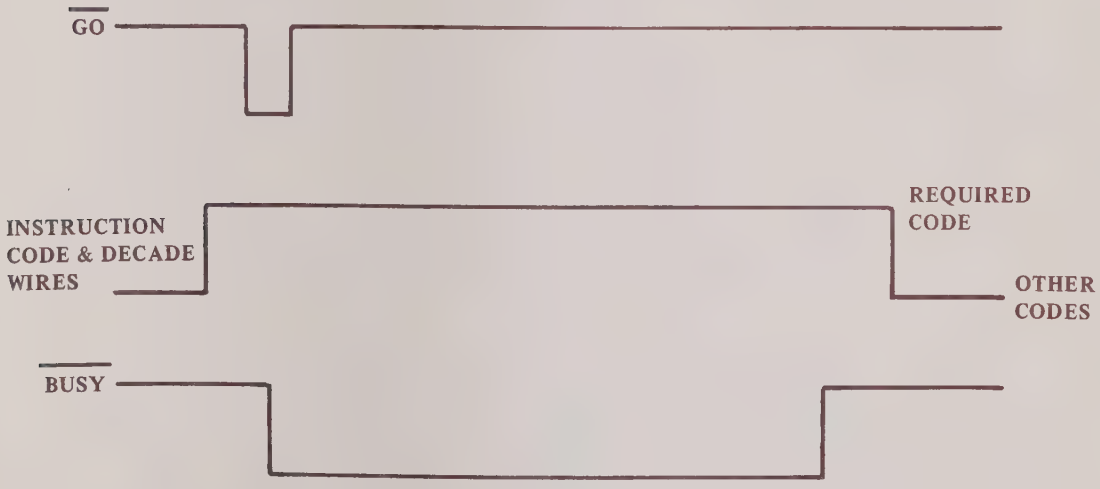
* In Measure bias mode, the output from the system under test is not multiplied by the heterodyning signal, as this is not necessary.



INTRODUCTION TO ARITHMETIC UNIT

The arithmetic unit is capable of performing 32 different operations. Some of these transfer information to or from the store. Some are simple calculations, such as an addition, and some are more complex, such as calculating the logarithm of a number. The most complex operation which can be performed autonomously by the arithmetic unit (in conjunction with the input system, the sin/cos generator and the N-cycle counter) is the correlation process itself (the operation performed by the arithmetic unit during the correlation process is termed "integration"). More complicated calculations are made up of sequences of instruction, which are commanded in turn by the control logic.

The control logic produces a 6 wire instruction code to the arithmetic unit. Five of these wires specify which of the 32 instructions the arithmetic unit is to perform. When the code has been set up, the control logic issues a $\overline{GO}$ pulse to the arithmetic unit, which is the command to start the specified operation. When the $\overline{GO}$ pulse has been accepted, the arithmetic unit returns a $\overline{BUSY}$ signal to the control logic. This inhibits further control logic action until the arithmetic unit operation is completed. The arithmetic unit then performs the operation. This may take 2μSec for a single addition, or several hours for a long integration. When it has finished it removes the $\overline{BUSY}$ signal to the control logic, which then continues to the next instruction in the program.



Arithmetic Unit Command Sequence

Some arithmetic unit operations make use of a decade number. This is produced by the control logic before the $\overline{GO}$ pulse, as a 3 wire binary number.

After an arithmetic unit operation, the control logic can use conditional instructions to sense various conditions in the arithmetic unit.

The arithmetic unit communicates data via a 4 wire static data bus. This allows it to transfer 4 bit numbers between registers within itself, or to and from the store. When communicating with the store, data is transferred between the arithmetic unit data bus (static) and the store data bus (dynamic i.e. changing every 2μSec) by an interface on Board 11, which is controlled by the control logic. Three "enables" wires, which are produced by the control logic, control which of the three registers in the arithmetic unit is allowed to write onto the data bus.

The signals described are sufficient for the arithmetic unit to perform any of its 32 operations except for integration (and measure delay), which is described later.

ARITHMETIC UNIT INTERNAL ORGANISATION

The arithmetic unit proper (excluding parts used only for integration and measure delay) consists of the following parts:

1. Decode Logic	Translates 5 instruction code wires from the control logic into the 22 wires necessary to control the individual parts of the arithmetic unit. (These wires are all static throughout an operation)
2. Condition Multiplexer	Used to feed information about the contents of the registers etc. to the control logic.
3. Sequence Logic	Receives the $\overline{GO}$ pulse from the control logic and generates all sequential pulses and clocks required by the various parts of the arithmetic unit. A $\overline{BUSY}$ signal is returned to the control logic to prevent it continuing to the next instruction until the current one has finished.
4. Registers A & B	Both registers are identical. Each stores a 9 digit BCD number, with sign, and is capable of adding or subtracting another 9 digit number from it, in 1.8μSec.
5. Register C	This is also referred to as the iteration counter or timer counter. It is a 6 digit BCD up/down counter. The i/p clock can be applied to any of its 6 stages, thus changing the significance of each i/p pulse.
6. Exponent Counters	Exp A and Exp B are 4 bit counters, used to keep the exponents of the contents of register A and B during shift operation etc. They can be read by, or loaded from the store, via the data bus. An Exp C is also available and can be read by the store (it cannot be loaded). It is always equal to Exp B - Exp A.

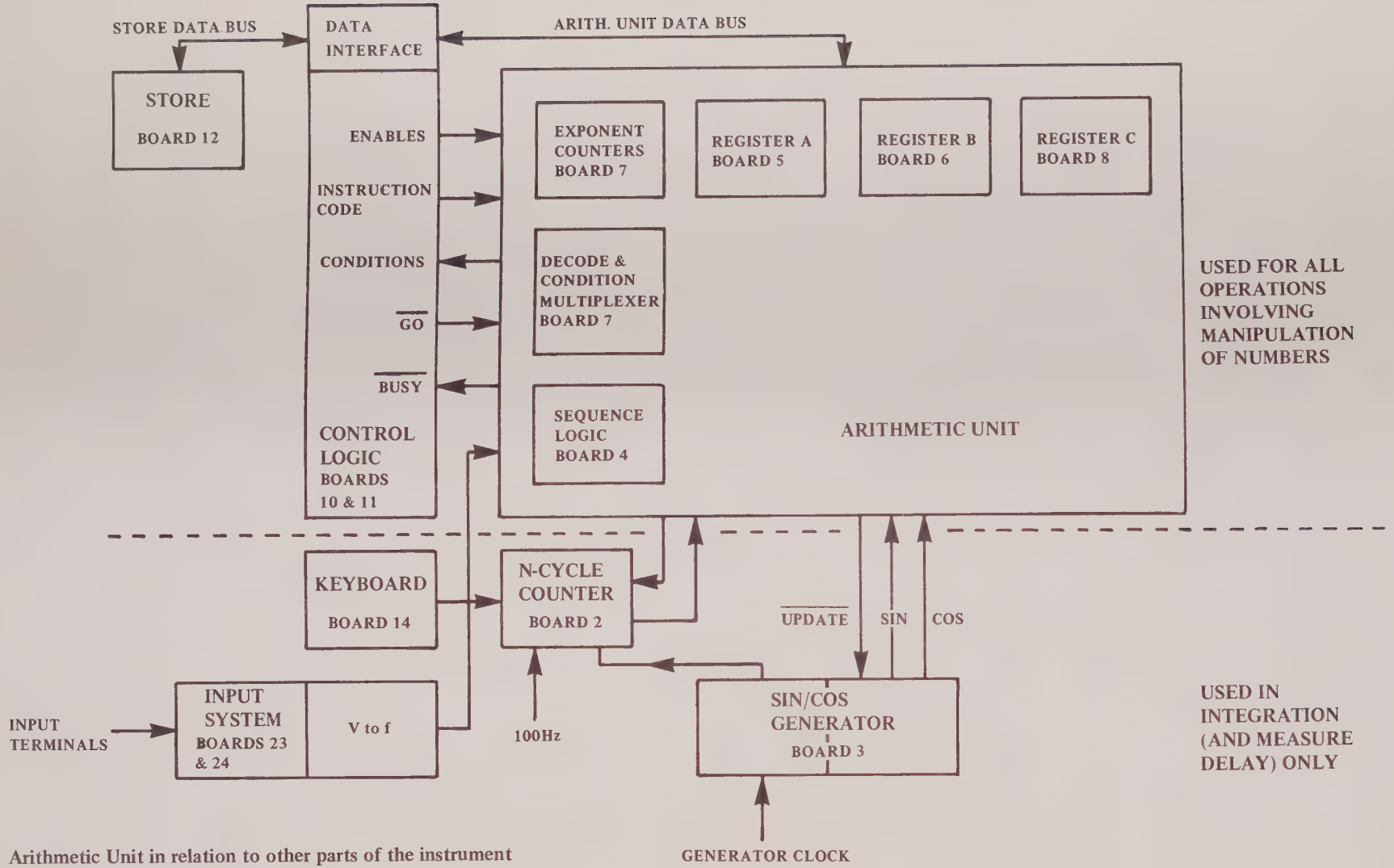
The arithmetic unit operates in "cycles". Each cycle takes 1.8μSec. Some arithmetic unit operations take only one cycle (e.g. an addition or a transfer of one digit between a register and the data bus), others may take up to 2 or 3 thousand cycles (e.g. calculating a logarithm) whilst integration may take a more or less unlimited number of cycles.

Registers A and B can each store a 9 digit BCD number, and a sign, indefinitely. The most significant digit is an overflow digit, and is known as the 9th digit. The remaining digits are numbered from 0 (most significant, except for the 9th digit) to 7 (least significant). In a single cycle, either or both registers can add or subtract another 9 digit number (the "input data") from the current contents of the register. The answer becomes the new contents. More complex operations are made up of many such cycles, each consisting only of additions or subtractions. Each register can select one of a number of sources from which the input data may come. Each register produces 3 output signals which may be used as input data either by itself or by the other register. The outputs are equal to:

(a)	the register contents	A	B
(b)	the register contents x10	10A	10B
(c)	the register contents ÷ 1000	A/1000	B/1000

Input data may also come from other sources (data bus, sin/cos generator, or log constant from board 4). The registers may add none, some or all of the 9 digits of the input data. The number may be added to the current register contents, or the current contents may be discarded and the input data added to zero. Different combinations of these alternatives produce all possible types of cycle which the arithmetic unit can perform.

The various cycle types are described in Table A.



Arithmetic Unit in relation to other parts of the instrument

REGISTER A

SEE NOTE NO.	DIGITS OF INPUT DATA ADDED 9th 0 1 2 3 4 5 6 7	ADD/SUB	SOURCE OF I/P DATA	ADDED TO
1,11			Zero	Current conts.
2			Zero	Zero
2		+	Register A	Zero
3			Zero	Current conts.
3			Zero	Current conts.
3		+	Register B	Current conts.
3		-	Register B	Current conts.
4		+	Register A	Current conts.
4			Zero	Current conts.
5		+	Register B	Zero
6		-	Register A	Zero
7			Register A	Zero
8		+	10A	Zero
8		+	Register A	Zero
9		-	10A	Current conts.
10		+	Data bus	Current conts.
10			Zero	Current conts.
12		-	Log const.	Current conts.
13		+	Log const.	Current conts.
14		+	B/1000	Current conts.
15		-	B/1000	Current conts.
16			Zero	Current conts.
16			Zero	Current conts.
17			Zero	Current conts. ÷ 10
18			Sin "1" digit	Current conts.
			Sin "10" digit	Current conts.

The ADDED TO column refers to **both** registers. The contents of register A after an operation is the sum (or difference) of the SOURCE OF INPUT DATA (Reg A) column and the ADDED TO column. Thus for AAdd, the contents of register A after the operation is Register B + Current conts of Register A. Similarly for register B.

The DIGITS OF INPUT DATA ADDED column shows which digits of the input data are added to (or subtracted from) the register. Thus the data bus is added to one digit only, in a Load operation, and the least significant 6 digits only of the B/1000 signal are used in a Log operation.

REGISTER B

DD/SUB	SOURCE OF I/P DATA	DECADE NO.	INSTRUCTION NAME	CODE	NOTES
	Zero		Read	12	Also used for CLoad, AExp dec, BExp dec
+	Register B		AClear	8	
	Zero		BClear	9	
+	Register A		BAdd	0	
-	Register A		BSub	1	
	Zero		AAdd	2	
	Zero		ASub	3	
	Zero		ADouble	19	
+	Register B		BDouble	20	
+	Register A		Swap	21	
+	Register B		AInv	17	Subtracts Register A from zero, forming 10s complement
	Register B		Complement	18	Subtracts either register from zero if it is negative
+	Register B		ATen	29	Shifts register A one decade up
+	10B		BTen	30	Also used for CTen. Shifts register B one decade up
	Zero		Ax-9	16	Multiplies register A by -9
	Zero	0	ALoad	10	Also used for AOne load
		1			
		2			
		3			
		4			
		5			
+	Data bus	0	BLoad	11	Also used for BOne load
		1			
		2			
		3			
		4			
		5			
+	B/1000		Log	4	
-	B/1000		Exp	5	
-	A/1000		Polar	6	
+	A/1000		Cartes	7	
-	Register A		XDivide	22	} Iterative operations (10 cycles max) used in the division routine.
+	Register B		YDivide	23	
	Zero		DTen	26	Shifts both registers one decade down.
	Cos "1" digit Cos "10" digit		} Int	24	

NOTES

SINGLE CYCLE OPERATIONS

1. Registers A & B are each equipped with an "output latch", which is used when a digit is read from the register onto the data bus. Digits 0 to 5 may be read onto the bus. If one of these is selected by the "decade" wires (from the control logic), it is entered into the output latch during any cycle performed by the arithmetic unit, of whatever type. The contents of the latch are read onto the data bus when the "enable" wire (from the control logic) for the register is high. Normally the sequence to read a digit consists of setting up the decade wires to the desired digit number, performing a "read" operation in the arithmetic unit, and enabling the register which is to be read. The desired digit is then present on the data bus and may subsequently be loaded into another register, or the store.

The "read" operation does not alter the contents of either register. Its function is to ensure that the desired digits are entered into the output latches.

It is also used for certain auxiliary operations which affect only the exponent counters or register C. Signs and exponents, and data in register C, are read onto the data bus immediately their decade number and enable wire are set up (i.e. they do not require a cycle to "latch" them). However, for the sake of uniformity, a "read" operation is normally performed as for digits 0 to 5 of registers A and B.

For the purpose of communication via the data bus the signs are allocated decade number 6 (+ve = value 0, -ve = value 1) and exponents decade number 7.

2. **Clear** operations clear all 9 digits of the register in question to zero. The signs and exponents are unaffected by a clear operation. In order to clear them it is necessary to load zero into them from the data bus. This is also true of register C (there is no CClear operation).

3. **Additions and subtractions** are single cycle operations. They are full 9 digit calculations. Carries and borrows out of the 9th decade are lost. The sign bistables will follow changes of sign correctly only if negative numbers are in 10's complement form before the addition or subtraction. Answers will then also be in 10's complement form if negative. If the signs are not of interest, additions and subtractions may be performed on numbers in "absolute value and sign" form - the operation will take place on the absolute values, the result will be complemented if the difference in absolute values (in a subtraction) was negative, and the signs will not have any straightforward meaning after the operation.

4. "**Double**" operations are performed by adding the number to itself. Signs are unaffected, and carries out of the 9th decade are lost.

5. A "**Swap**" operation adds the contents of register A to register B, and the contents of register B to register A. The input data is added to zero in each register. Signs and exponents are unaffected (i.e. they are NOT swapped).

6. An "**AInvert**" operation subtracts the contents of register A from zero. Register B and both signs are unaffected.

7. **Complement**. The register are set up as if they were each to subtract their current contents from zero. However, gates on boards 5 and 6 ensure that they are subtracted if negative, and added if positive. The 10's complement is thus formed. Signs are unaffected. This operation is used to convert numbers in "absolute value and sign" form to 10's complement form and vice versa.

8. **ATen, BTen, and CTen** operations add the current contents x10 to zero in one register, the the contents of which are thus shifted up one decade, and add the contents to zero in other register, which is thus unaffected. The 10A and 10B signals are formed by a circulair shift process, so that the 9th decade of the contents of register A becomes digit 7 (least significant digit) of signal 10A. Signs are unaffected by the operation. In ATen and BTen operations, the exponent of the register being shifted is reduced by one, to keep the magnitude represented by the register constant. Exponents are not affected by CTen (this is the only difference between BTen and CTen).

9. The **Ax-9** operation subtracts 10A from A, giving a result -9A. In conjunction with AInvert, this enables numbers to be multiplied by 9, which is useful in calculating degrees from radians. Register B, signs and exponents are unaffected by the operation.

10. **ALoad and BLoad.** These operations add the data present on the data bus to the register, in one digit position only between 0 and 5. It is not necessary for the register to contain zero before the operation - input will be added correctly (loading of register A and B is additive). If digits 6 (sign) or 7 (exponent) are addressed, the contents of the register will remain unchanged, but the data present on the data bus will replace the current contents of the sign bistable or the exponent counter of the register in question (loading of signs and exponents is destructive). The 9th digit 6 and7 of the registers themselves cannot be loaded from or read onto the data bus.

11. **CLoad.** One of digits 0 to 5 of register C may be loaded from the data bus by a CLoad operation. This is accompanied by a "read" operation which has no effect on the contents of register A and B. Loading of results C is *destructive* - no CClear operation is provided. If digit 6 or 7 is addressed, the CLoad operation has no effect at all.

ITERATIVE OPERATIONS

Outputs are provided from registers A and B to show when a carry or borrow from digit 0 into the 9th decade has occurred. An output is provided from register C to show when it has counted to state zero, either by overflowing (when counting UP) or by counting DOWN to zero. Circuitry is provided (Board 4) so that when commanded to "go" by the control logic, the arithmetic unit will perform cycles continuously until one of the above three things happens. The arithmetic unit then returns control to the control logic by removing the $\overline{\text{BUSY}}$ signal. Counting to zero in register C will always terminate an iterative operation. Some iterative operations are also terminated by a carry or borrow in either register A or register B.

12. **Log.** In a cycle of a "log" operation, B/1000 is added to the current contents of register B. This has the effect of multiplying the contents of register B by 1.001. A constant (log const.) equal to log 1.001 (= .00043402) generated on board 4, is subtracted from register A.

Since the B/1000 signal is generated by a circular shift process, the least significant three digits of B appear as the most significant 3 digits of B/1000, which should all be zero. Therefore in operations involving the B/1000 and A/1000 signals, only the least significant 6 digits of the input data are added to the registers.

The log operation commences with the number whose log is to be found in register B. Its most significant digit must be in digit 0 position (i.e. the number must be "normalised"). Register A contains zero, or a digit in the 9th decade only. Cycles of the type described above are then executed continuously until the signal indicating a carry into the 9th decade of register B appears. When this is received by the sequence logic (Board 4) it terminates the operation and removes the $\overline{\text{BUSY}}$ signal to the control logic, which continues to the next instruction in the program.

If we treat the decimal point of the registers as being between the 9th decade (integer part) and the rest of the register (fractional part), then the function of the log operation is to determine how many times it is necessary to multiply the initial value B ($1 > B \geqslant .1$) by 1.001 in order to make it $\geqslant 1$. This number is equal to the number of cycles performed, N.

This gives:

$$1 \approx B \times 1.001^{N}$$

taking logs: $0 = N \log 1.001 + \log B$

Simultaneously, the number $-N \log_{10} 1.001$ is calculated in register A, by subtracting the log constant, .00043402 (= log 1.001) from it once for each cycle performed.

Therefore:

A (final value of register A) $\approx$ - N $\log_{10}$ 1.001

substituting for N log 1.001 from above : $A \approx \log_{10} B$

Signs and exponents are not affected by this operation. Register C counts the number of cycles performed. This used as a safety measure to ensure that the operation will stop after 10000 cycles if an attempt is made to find the log of zero.

13. **Exp.** This operation is used to calculate antilogs. The operation starts with the number whose antilog is to be found in register A, and 1.0 in register B. The process is exactly the same as the log process, except that the log constant is *added* to register A, and the signal B/1000 *subtracted* from register B each cycle. The iteration continues until there is a carry into the 9th decade of *register A*.

This is equivalent to the calculation:

$$N = \frac{-A}{\log(1.001)}$$

$$B = 1.0 \times (.999)^N$$

hence: $N \log(1.001) = -A$

$N \log_{10} .999 \approx A$ since log 1.001 $\approx$ -log .999

taking antilogs: $(.999)^N \approx 10^A$

$B \approx 10^A$ (i.e. antilog A)

where A = initial value of register A
B = final value of register B
N = number of cycles performed

Signs, exponents and the contents of register C are not affected by this operation. It cannot continue for longer than 1/.00043402 (= 2305) cycles, regardless of the initial contents of the registers.

14. **Polar.** In a cycle of the "polar" operation, the B/1000 signal is added to register A, and the A/1000 signal subtracted from register B. The operation continues until a borrow from the 9th decade of B occurs (i.e. register B becomes negative). The number of cycles performed is counted by the iteration counter (register C). At the beginning of this operation, register A contains the "in-phase" component of the result of the measurement, register B the "quadrature" component, and the iteration counter contains zero. Each cycle is equivalent to rotating the vector represented by A and B towards the real axis by an angle of .001 Radians. This continues until the "quadrature" component becomes zero. At this point, the real part of the vector (the contents of register A) is equal to its amplitude, R, and the angle through which it has been rotated (i.e. the contents of the iteration counter) is equal to its phase angle, θ. Signs and exponents are not affected by this operation.

As for "Log", the operation will be terminated by the iteration counter after 10000 cycles if an attempt is made to convert a zero vector to polar form. The maximum number of cycles which can legitimately occur (corresponding to a rotation of 90^o) is $1000\pi/2$ (= 1571).

15. **Cartesian.** This operation is the reverse of "polar". Cycles are the same as cycles of the polar operation except that the B/1000 signal is *subtracted* from register A, the A/1000 signal is *added* to register B, the iteration counter counts *down* one for each cycle, and iterations continue until the iteration counter reaches zero. The operation starts with the vector amplitude (R) in register A, zero in register B, and the phase angle (θ), in milliradians, in the iteration counter. The operation consists of rotating the vector away from the real axis, in 1 milliradian steps, through an angle θ. Registers A and B are then equal to the "in-phase" and "quadrature" components of the vector.

A borrow occurring in register A will also terminate the "Cartesian" operation. This is a safety measure, as if register A became negative it would be in complement form, which could cause large errors in register B if the process were allowed to continue. The characteristics of this process are such that register A can become negative slightly before the vector has been rotated through 90° (the maximum allowed). Signs and exponents are not affected by this operaton.

16. **XDivide, YDivide.** These operations are used in the division routine. In the XDivide operation, the contents of register A are subtracted from the contents of register B repeatedly until register B become negative. The number of cycles performed is counted in the addressed decade of the iteration counter. The division routine is arranged so that the contents of register B are always less than 10 times the contents of register A before the XDivide operation. The maximum number of iterations performed is thus 10. The YDivide operation is exactly the same, except that register A is *added* to register B until it becomes *positive,* and the iteration counter counts *down* instead of up.
Signs and exponents are not affected by these operations.
For a more complete description of the division routine, see "THE 1170 SOFTWARE".

17. **Decsh.** Within each of registers A and B, it is possible to perform a circular shift of the digits, so that the contents of the registers are divided by ten. Since this circular shift operation would result in the least significant digit of the old register contents becoming the most significant digit of the new contents, this digit is gated out so that it is always zero after a Decsh operation. This is accomplished internally by the registers when commanded to operate in DECSH mode. Signs are not affected by the operation, and the exponents are both increased by one, to keep the magnitudes of the numbers being represented by the registers constant.

18. **Integrate.** In a single cycle of the integrate operation, the least significant digit (the "1" digit) of the "sine" signal, from the sin/cos generator, is added to or subtracted from the least significant digit of register A, and the least significant digit of the "cosine" signal added to or subtracted from the least significant digit of register B. Then (within the same cycle) the source of the input data is changed to the most significant digits (the "10" digits) of the "sine" and "cosine" signals, and these are added to or subtracted from the next digit in the registers (digit no. 6). Carries or borrows into the remaining 7 digits of the registers can occur, but no data is added.

Exponents are not affected by the "integrate" operation, but the signs follow the signs of the registers. These may change many times during a complete integration. For a more complete account of the integration operation, see "THE CONTROL OF INTEGRATION".

INTRODUCTION TO BOARD 3

The circuitry housed on board 3 can conveniently be divided into 4 sections as follows:

SIN/COS GENERATOR
DIVIDE BY 10/51 COUNTER
SET 0^{o} LOGIC
CHOP SIGNAL GENERATOR

These sections are used only during the integration section of each measurement sequence.

SIN/COS GENERATOR

This section receives a clock (SIN/COS CLOCK) from the divide by 10/51 counter. This clock has 200 pulses per correlator cycle. In response, the sin/cos generator produces two signed 2 digit BCD numbers representing sin $2\pi ft$ and cos $2\pi ft$, which are fed to arithmetic registers A and B respectively (boards 5 & 6).

DIVIDE BY 10/51 COUNTER

The divide by 10/51 counter has as its input the generator clock and produces as its output the sin/cos clock.

At frequencies below 1kHz, the correlator and generator run at the same frequency, f. The generator clock (2000f) is divided by 10 to produce the sin/cos clock at frequency 200f.

At frequencies $\geqslant$1kHz, the correlator operates in the "heterodyne" mode. The generator clock (200f) is divided by 51 to produce the sin/cos clock at frequency 200f/51. A further divide by 4 counter produces the heterodyning signal (50f/51).

The sin/cos clock is wire-OR-able, enabling the correlator frequency to be modified. This is used in particular by the 1185 Harmonic Analysis option, which adds clock pulses to the sin/cos clock, causing the correlator to run at a multiple of its fundamental frequency.

The basic sin/cos clock (before wire-OR-ing) is fed to the n-cycle counter (renamed N-CYCLE CLOCK), so that integration is always for a whole number of cycles of the correlator *fundamental* frequency.

SET 0^{o} LOGIC

The correlator must be set to 0^{o} whenever one of the following two cases apply.

(a) when the generator passes through 0^{o} (or $\geqslant$1kHz, every 51 times the generator passes through 0^{o}) and,

(b) when the external world sets the generator to 0^{o}.

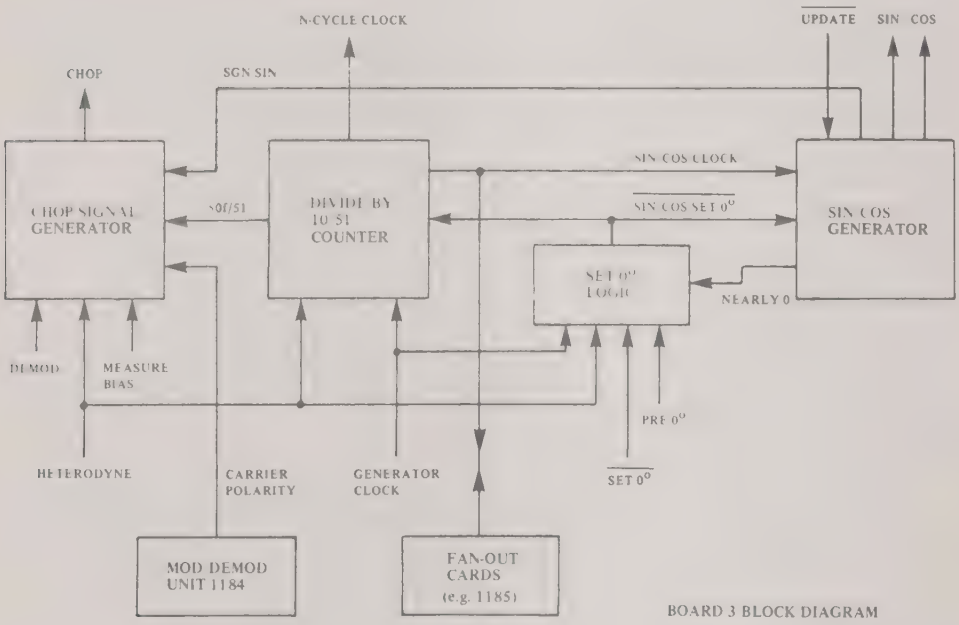
Case (a) is indicated by the PRE 0^{o} signal and case (b) by the $\overline{\text{SET } 0^{o}}$ signal. The SET 0^{o} logic combines these two signals, disables 50 out of 51 0^{o} pulses if f $\geqslant$1kHz, and produces a signal $\overline{(\text{SIN/COS SET } 0^{o})}$ to set the sin/cos generator and the divide by 10/51 counter to the 0^{o} state.

CHOP SIGNAL GENERATOR

The input system requires a square wave signal (CHOP) by which to multiply the input signal when not in its basic mode. When the machine is heterodyning the 50f/51 signal is used; when demodulating, the carrier polarity signal (CARRIER POS) is used and when measuring bias the correlator polarity signal (SGN SIN) is used.

The machine can be doing more than one of these things at once (e.g. measuring carrier bias, in which case both the DEMOD and MEAS BIAS modes are used, or demodulating above 1kHz where DEMOD and HETERODYNE modes are used).

The chop signal generator selects and combines the required signals, stretches any resulting pulses which are too short for transmission through a pulse tranformer, and feeds the signal (CHOP) to the input system.



BOARD 3 BLOCK DIAGRAM

INTRODUCTION TO BOARD 8

Board 8 houses "Register C", also known as the "iteration counter" or "timer counter". Its function is to count the cycles performed in an iterative operation (LOG, POLAR, CARTES, or a step in the division routine, XDIVIDE, YDIVIDE), and to measure the time taken by the integration operation.

It consists of the following functional blocks:-

COUNTER

This is a 6 digit, synchronous, up/down counter (IC7 to 12, plus associated gates). The mode of the counter (UP or DOWN) is controlled by a wire from the Decode logic (board 7). The counter is arranged so that the clock may be applied to any of its 6 digits, thus altering the "significance" of the clock. This is controlled by the three decade wires.

DECADE No.	CLOCK SIGNIFICANCE
0	100,000 bits
1	10,000 bits
2	1,000 bits
3	100 bits
4	10 bits
5	1 bit
6 or 7	0 (no count)

Digits less significant than the addressed digit are not affected by the clock. Carries or borrows into digits more significant than the addressed digit occur normally.

Example

Decade No. = 3
UP/DOWN = UP

Initial contents	005741
After 1 clock pulse	005841
2	005941
3	006041
4	006141
	etc.

Any one of the 6 digits of the counter may be loaded from the data bus. If the LOAD C wire (from Decode logic) is high, a pulse on the ITERATION CLOCK wire, which occurs once for each cycle performed by the arithmetic unit, will cause the digit on the data bus to replace the addressed digit in the counter. The old digit is lost. Unaddressed digits are not affected by a load operation. If the decade number is 6 or 7, none of the digits are affected. A CLoad operation (see Decode logic truth table) consists of a "read" cycle, which does not affect the contents of registers A or B, performed with the LOAD C wire high.

DATA OUTPUT MULTIPLEXER

Any one of the 6 digits of the counter may be read onto the data bus. The multiplexer section receives the data from each of the 6 digits, selects the output from the addressed digit (if the decade number is between 0 and 5) and reads it onto the data bus if the ENABLE C line (from the control logic) is high. The multiplexer section consists of 6 sets of 4 gates (IC1 to 6) which are wire-OR-ed together, a set of "enable" gates (IC22) and a set of 4 drivers for the data bus (IC24).

CLOCK CONTROL

This section consists of IC27a and IC25c.

During single cycle operations, the iteration counter is not affected. In this case the ITERATE wire and the INTEGRATE wire (from Decode logic) are both low, and the counter receives no clock.

During iterative operations, the counter is required to count the number of cycles performed. In this case the ITERATIVE wire is high, and the counter counts the number of pulses on the ITERATION CLOCK wire, which is equal to the number of cycles performed by the arithmetic unit.

During integration, the counter is required to measure the time of integration. The INT wire is high, and the ITERATE and the $\overline{\text{BUSY}}$ wires low. The counter thus counts $\overline{\text{TIMER CLOCK}}$ signal (see "CONTROL OF INTEGRATION").

OVERFLOW BISTABLE

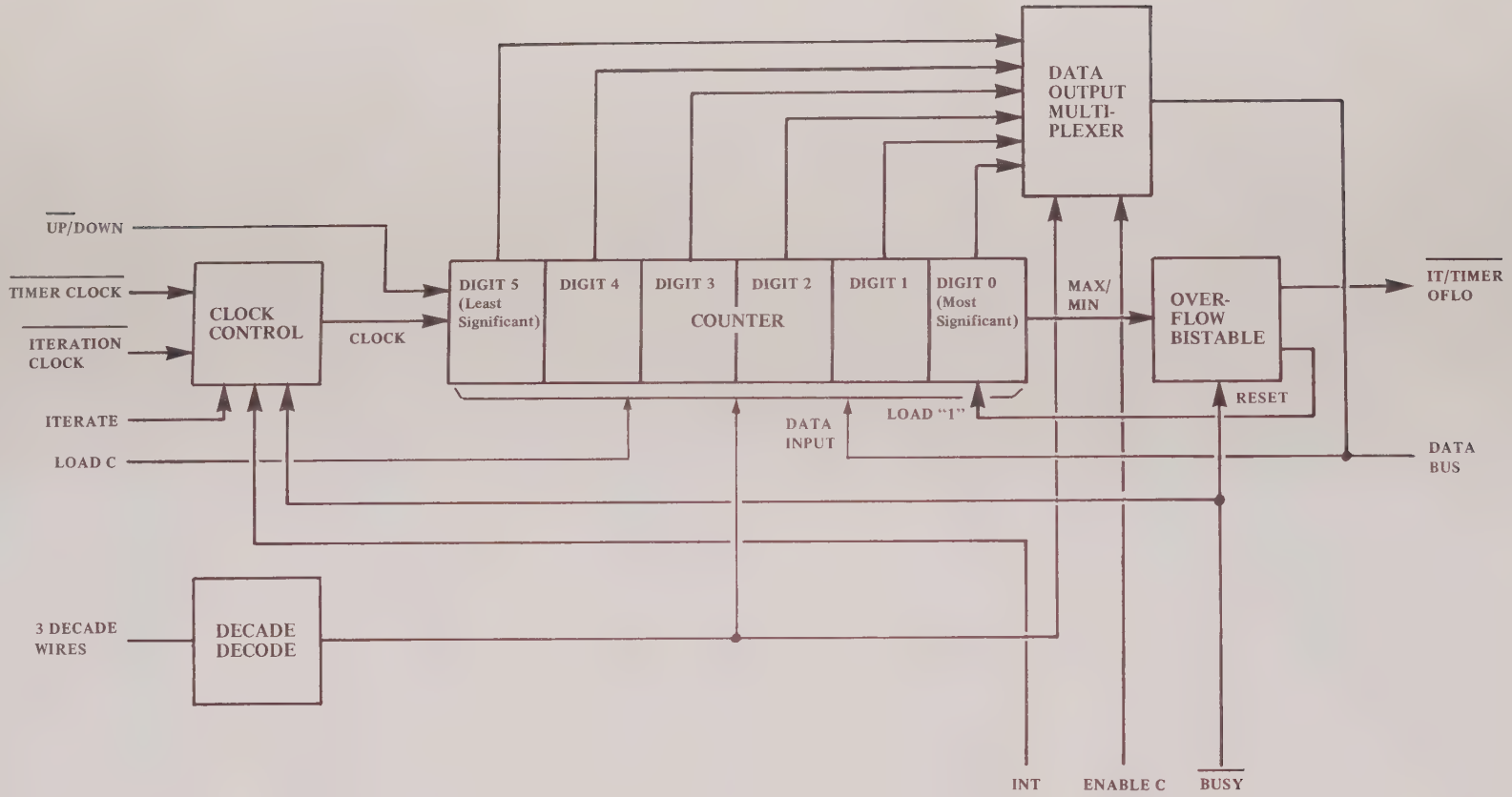
This section produces an output ($\overline{\text{TIMER/ITERATION OVERFLOW}}$) to the sequence logic whenever the part of the counter which is selected counts to zero, either by overflowing (when counting UP) or by counting DOWN to zero. This is used, during iterative operations, to terminate the operation, or, during integration, to initiate an INT.DECSH operation (see "CONTROL OF INTEGRATION"). The signal is derived from the MAX/MIN output from the most significant digit of the counter.

The signal is derived from the MAX/MIN output from the most significant digit of the counter. This is used directly when the counter is counting DOWN (the state zero is the MIN state, i.e. the state immediately before overflow) but is delayed by one clock pulse by a bistable (IC28) when counting UP, as the state zero is reached one pulse *after* the MAX state (i.e. it is the state immediately *after* overflow). The bistable is reset by the $\overline{\text{BUSY}}$ signal at the beginning of every operation.

This section consists of IC28, IC27b, IC20d and e, IC25d and IC23c. Logic is provided so that, during integration (when the INT wire is high), an overflow causes a "one" to be loaded into the most significant digit of the counter. Whenever INT is high, the number "one" is placed on the data inputs of IC12 (this is accomplished by IC18c and IC21b, c and d). When an overflow occurs, a pulse appears on the LOAD input of IC12 (pin 11), causing "one" to be loaded, (accomplished by IC19b). During integration, the counter goes through the states:-

999998
999999
100000
100001
100002
etc.

For a fuller description of this process, see "CONTROL OF INTEGRATION".



BOARD 8 BLOCK DIAGRAM
(for more detail refer to circuit diagram)

EXPONENT COUNTER

The exponent counter is situated on board 7. It consists of two 4-bit up/down counters (IC10 and 11), which are used to keep track of the exponents of the contents of registers A and B during shift operations etc. They are known as "Exp A" and "Exp B" respectively. Each of them may be read onto or loaded from the data bus. Two explicit arithmetic unit operations are provided to decrease the contents of either Exp A or Exp B by one ("AExp dec" and "BExp dec"). The operations ATen and BTen also cause the contents of Exp A and Exp B respectively to be decreased by one, in addition to shifting the contents of registers A and B. The operation DTen causes the contents of both Exp A and Exp B to be increased by one, in addition to shifting the contents of registers A and B. If an attempt is made to increment an exponent counter from state 15, it will overflow, and the subsequent state will be zero. The carry out of the counter is lost. Similarly, when counting down, the counters will underflow from zero to 15, and the borrow out of the counter will be lost.

The magnitude of Exp A-Exp B is calculated by a 4-bit adder (IC9) and a set of inverters (IC13) and can be read onto the data bus as Exp C. It cannot of course be loaded explicitly. The sign of Exp C, and a signal which detects that Exp C = 0 (i.e. Exp A = Exp B), can be sensed, via the condition multiplexer, by the control logic. When Exp C is negative (i.e. Exp A > Exp B) it is expressed in 2's complement form.

DETAIL

Loading

If STROBE A and LOAD are high, and the decade number is 7, a pulse on the $\overline{\text{ITERATION CLOCK}}$ wire (which occurs once for every cycle performed by the arithmetic unit) will cause a pulse to appear on the "load" input of IC11 (pin 11) and the digit present on the data bus will replace the current content of Exp A. The old contents are lost (loading of exponent counters is *destructive*). Since an ALoad operation with decade 7 selected will have no effect on register A, Exp A may be loaded exactly as if it were a digit of register A, which is allocated decade number 7.

Loading of Exp B is an exactly analogous process.

Reading

The exponent counters are read onto the data bus via two Quad 2 to 1 line multiplexers (IC8 and IC15). One of Exp A (IC11), Exp B (IC10) or Exp C (IC9) is selected according to the state of the Enable wires (only one of which may be high at a time). It is only read onto the data bus if the decade number is 7. The exponent counters can thus be read exactly as if they were digits in the registers which are allocated decade number 7. It is not necessary to perform a "read cycle, but the control logic does so for the sake of uniformity, and to initiate a data transfer to the store via the store-arithmetic unit data interface.

Counting

The DECSH CMD wire is used as the up/down control wire for both counters. The $\overline{\text{ITERATION CLOCK}}$ signal is used as the clock - the counters are thus incremented or decremented by one for each cycle performed in which they are enabled. Exp A is enabled (by IC20c) if either the ATEN or DECSH CMD wires are high, and Exp B is enabled (by IC20d) if either the BTEN or DECSH CMD wires are high.

Condition Outputs

The sign of Exp C is simply the "carry" output of the adder which computes Exp C. This is the signal EXP C POS. Zero is detected by IC16 a and b and IC17d - this is the signal $\overline{\text{EXP C ZERO}}$.

DECODE LOGIC

The various parts of the arithmetic unit have a total of 22 control wires, the state of which determines the operation which is performed when the arithmetic unit is commanded to "go". Each of these wires is static throughout an operation - they must be set up before the arithmetic unit receives the $\overline{GO}$ pulse, and must remain set up until the operation is completed (i.e the arithmetic unit removes the $\overline{BUSY}$ signal).

The arithmetic unit can perform 32 different types of operation, each of which is allocated to a particular state of the 5 "instruction code" wires, by which the control logic controls the arithmetic unit, and each of which requires that the 22 control wires are set up to a particular state. The 32 different states of the 5 instructions codes wires are translated into the corresponding 32 states of the 22 control wires by the Decode Logic.

This is situated on board 7, and comprises two 256 bit read only memories, (IC1 and 2), each of which receives the 5 instruction code wires as its address and produces 8 of the 22 control wires. The remaining 6 of the control wires are produced by a one-in-ten decoder (IC3, type 7442) and a number of gates.

The truth table for the Decode Logic, together with the instruction names and the names of the 22 control wires is shown in Table A.

TABLE A DECODE OUTPUTS

INSTRUCTION CODE	IC1								IC2								IC3						INSTRUCTION NAME
	1/1000	$\overline{\text{CLEAR}}$	LOAD	STOP CODE B	STOP CODE A	STROBE B .	STROBE A	$\overline{\text{INH}}$ SGN CH	MPX 1 CMD	MPX 2	MPX 4A	MPX 4B	ADD B CMD	ADD A CMD	$\overline{\text{UP}}$/DOWN	ITERATE	INT	DELAY/$\overline{\text{INT}}$	LOAD C	DECSH	ATEN	BTEN	CONTROL SIGNAL
0	0	1	0	1	1	1	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	BAdd
1	0	1	0	1	1	1	0	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	BSub
2	0	1	0	1	1	0	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	AAdd
3	0	1	0	1	1	0	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	ASub
4	1	1	0	1	0	1	1	0	1	0	1	1	1	0	0	1	0	0	0	0	0	0	Log
5	1	1	0	0	1	1	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	Exp
6	1	1	0	1	0	1	1	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	Polar
7	1	1	0	0	1	1	1	0	0	0	1	1	1	0	1	1	0	0	0	0	0	0	Cartes
8	0	0	0	1	1	1	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	AClear
9	0	0	0	1	1	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	BClear
10	0	1	1	1	1	0	1	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	ALoad
11	0	1	1	1	1	1	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	BLoad
12	0	1	0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	Read
13	0	1	0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	1	0	AExp dec
14	0	1	0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	BExp dec
15	0	1	1	1	1	0	1	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	AOne load
16	0	1	0	1	1	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	AX-9
17	0	0	0	1	1	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	AInv
18	0	0	0	1	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Comp
19	0	1	0	1	1	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	ADouble
20	0	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	BDoubie
21	0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	Swap
22	0	1	0	1	0	1	0	0	0	1	1	1	0	1	0	1	0	0	0	0	0	0	XDivide
23	0	1	0	1	0	1	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	YDivide
24	0	1	0	1	1	1	1	1	0	0	0	0	1	1	0	0	1	0	0	0	0	0	Int
25	0	0	0	1	1	0	0	0	1	1	1	1	1	1	0	0	1	1	0	0	0	0	MDelay
26	0	1	0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	1	0	0	0	DTen
27	0	1	0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	0	CLoad
28	0	0	0	1	1	1	1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	CTen
29	0	0	0	1	1	1	1	0	1	1	0	1	1	1	0	0	0	0	0	0	1	0	ATen
30	0	0	0	1	1	1	1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	1	BTen
31	0	1	1	1	1	1	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	BOne Load

Condition Multiplexer

The control logic can sense the state of a total of 32 different wires in the instrument, by means of conditional instructions. The names and meanings of these wires are shown in INTRODUCTION TO THE CONTROL LOGIC, Table B. The sixteen wires in Group 2, which include all those originating within the arithmetic unit, appear on board 7, and are multiplexed to two wires by means of two 8-to-1 line multiplexers. The 8 wires with numbers between 0 and 7 are multiplexed onto the ARITH COND 1 wire by IC5. The 8 wires with numbers between 8 and 15 are multiplexed onto the ARITH COND 2 wire by IC6. Both of these multiplexers are addressed by the least significant three instruction code wires.

Arith Bistables

Two bistables are provided for use by the control logic as memory elements or as a counter. The bistables are arranged as a two-bit "down" counter, and are controlled by the 6th instruction code wire (the "32" bit of the instruction code). The counter is clocked by the $\overline{\text{BUSY}}$ signal only if this wire is high - it is thus clocked one for each arithmetic unit instruction with a code between 32 and 63 (these 32 codes are otherwise exact duplicates of the codes between 0 and 31).

The state of the least significant bistable (which changes state for every operation with a code between 32 and 63) can be sensed as condition 11, and the most significant bistable (which changes state when the least significant bistable changes from 0 to 1) can be sensed as condition 12. No means of resetting the bistable explicitly is provided.

Input System Settling Delay

A monostable (IC7) is provided for use as a delay after changing the input range (during the autorange sequence) or the input system mode (during a reject bias measurement) to ensure that the input system has recovered from any overload state before commencing a measurement. The monostable is triggered by a pulse output from the control logic ($\overline{\text{CMD DELAY}}$) and its output can be sensed as a condition 6. Its period is nominally 30mSec.

THE ARITHMETIC REGISTERS

Introduction

Most of the arithmetic performed by the arithmetic unit is accomplished by two registers, Register A and Register B. Each consists of an identical board, numbered 5, occupying positions 5 and 6 respectively in the instrument. They are referred to in this account as "the board" or "the register" (not to be confused with the term "shift register", which refers to a single integrated circuit), and where signal names are given they refer to Register A, with the corresponding name for Register B in brackets, if different.

Each board can store indefinitely a 9 digit BCD number, with sign, and can add or subtract another 9 digit number ("input data") from it. The board works on a "digit by digit" basis. The input data is added to the register contents one digit at a time, starting with the least significant digit. Each digit requires one clock pulse, to perform a complete addition or subtraction thus requires 9 clock pulses. Clock pulses always occur in groups of nine at a rate of 5MHz. Each group corresponds to an arithmetic unit "Cycle". Iterative operations are made up of many additions or subtractions, and thus require many cycles.

Data Timing

The least significant digit of the input data is accepted by the board on the first clock pulse of the cycle, and the most significant digit on the last clock pulse. All sources of input data must be timed accordingly. The least significant digit must be present before and until the first clock pulse (when it is accepted by any board that is using it as input data). It is then replaced by the second digit in readiness for the second clock pulse, and so on, until the ninth (last) clock pulse, when the most significant digit is accepted by the board, and is replaced by the least significant digit in preparation for the next cycle.

Control Wires

The board is controlled by a number of control wires. These can be divided into two groups:

a) Sequential control wires.
These originate on board 4 ("Sequence logic"), and may change pulse by pulse through the cycle. They include the clock signal mentioned above.

b) Static control wires.
Most of these originate on board 7 ("Decode logic"). They do not change during a cycle (or only at points in the cycle where they are not active).

These are detailed in Table 1.

a) Sequential control wires.

1. $\overline{\text{PRECLOCK}}$
2. $\overline{\text{CPO}}$
3. OUTPUT LATCH STROBE
4. MPX STROBE
5. MPX ADDR 1

b) Static control wires.

	REGISTER A	REGISTER B (if different)
1.	SGN V	
2.	SGN (SIN)	SGN (COS)
3.	ADD A CMD	ADD B CMD
4.	ADD B CMD	ADD A CMD
5.	POS B	POS A

6.	$\overline{\text{INH. SGN CH.}}$	
7.	LOAD	
8.	DECSH	
9.	DEC 6	
10.	$\overline{\text{CLEAR}}$	
11.	$\overline{\text{DEC 6}}$. $\overline{\text{DEC 7}}$	
12.	MPX ADDR 2	
13.	MPX ADDR 4A	MPX ADDR 4B
14.	STROBE A	STROBE B
15.	INT.	

TABLE 1

Data Communication

Data is communicated to and from the iteration counter or the store, one digit at a time, via the arithmetic unit data bus. This is a two directional, negative logic, four wire, data bus. Each register is provided with an "enable" wire. When the enable wire for a register is high, a previously selected digit is read from the register onto the bus, where it will remain until it has been accepted by the receiving device (this may take up to 512μ Sec. for the store). When the enable wire is low, a zero is read onto the bus (i.e. four logic highs, as the bus operates in negative logic), freeing the bus for use by other registers. The digit which is read onto the bus is selected by means of the three "Decade" wires.

Internal Organisation

With the single exception of the data output latch, the board is composed entirely of synchronous logic. All bistables and shift registers are driven by the same clock signal, which is derived by a single inverter from the $\overline{\text{PRECLOCK}}$ signal. The heart of the board is a loop consisting of four 8 bit shift registers, a set of four bistables, and a BCD processor section (See Fig. 1.). The processor is divided into two parts, each consisting of combinational logic only, which are separated by the set of bistables. The four shift registers operate in parallel, so that data is shifted out of them into the processor section four bits (one BCD digit) at a time. Each digit passes through the shift registers, through the first part of the processor and into the set of bistables, then through the second part of processor and back into the shift registers. There are nine stages in this loop, so that at the end of a group of nine clock pulses, each digit has returned to its "home" position, having passed through all nine stages, and through the processor.

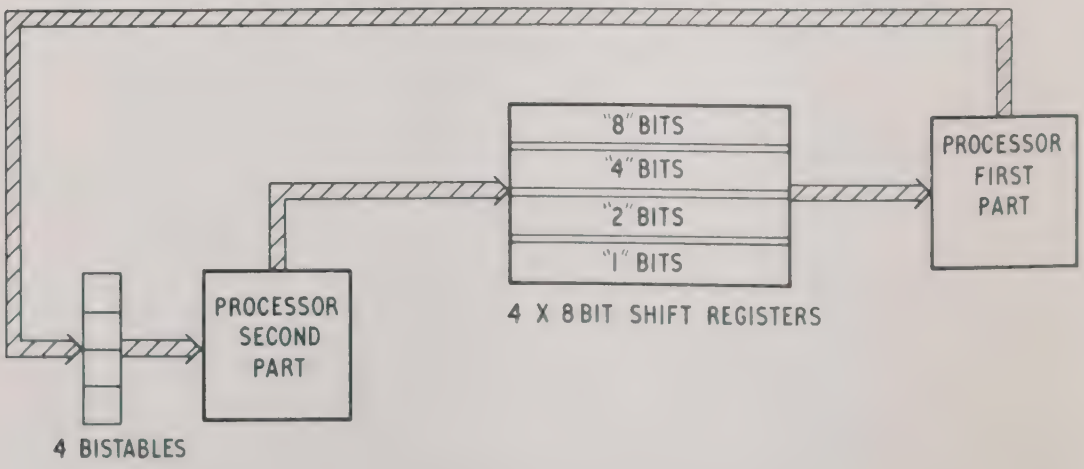


Fig. 1 Arithmetic Register Central Loop.

Processor (See Fig.2)

The first part of the processor performs a binary addition or subtraction of a digit of the data from the corresponding digit of the register contents, and computes the resulting decimal carry or borrow bit. Subtractions are performed by forming the ones complement of the input data (performed by a set of exclusive - OR gates) before it is added to the register contents. The intermediate result formed by the first part of the processor enters the set of bistables where it is stored until the next clock pulse. An "abnormal carry" bistable (ABN CARRY) stores the carry information and an ADD' bistable stores the add/subtract mode until the next clock pulse. A "carry/borrow" bit is computed from the outputs of these two bistables for addition to the next digit processed. No carry or borrow into the least significant digit is allowed - the "carry/borrow" bit is forced to the state marked "normal" when this digit is being processed (see table 2).

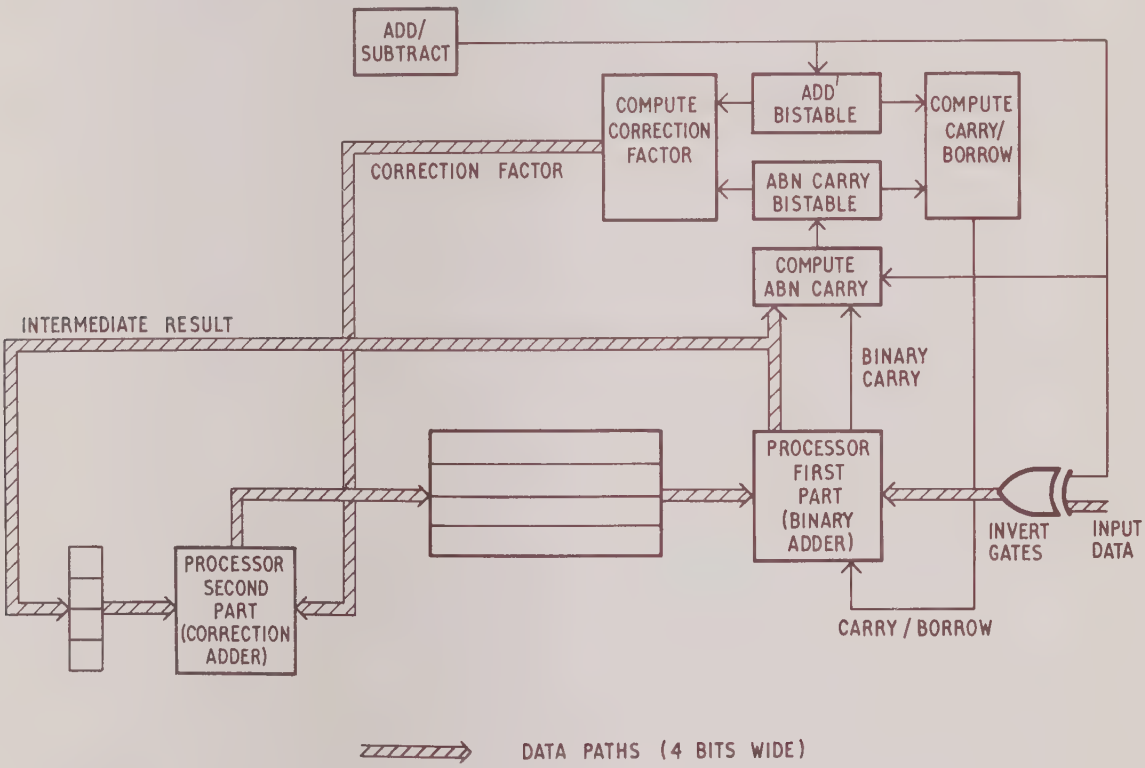


Fig. 2 Processor.

			CARRY/$\overline{\text{BORROW}}$	MEANING	ABN CARRY	CORRECTION FACTOR
ADD	sum <	10	0	normal	0	0
	sum ≥	10	1	carry one	1	6
SUBRACT	difference <	0	0	borrow one	1	10
	difference ≥	0	1	normal	0	0

TABLE 2

The second part of the processor is a "correction adder". It adds a correction factor computed from the output of the ABN CARRY and ADD bistables to the intermediate result, to give the final result. The "16" bit of this result is ignored, and it is then a true BCD digit (see table 3).

	ADD						SUBTRACT						
COLUMN	1	2	3	4	5		6	7	8	9	10	11	
	0	0	0	0	0		- 10	6	0	10	16	0)	
	1	0	0	1	1		- 9	7	0	10	17	1)	
	2	0	0	2	2		- 8	8	0	10	18	2)	
	3	0	0	3	3		- 7	9	0	10	19	3)	
	4	0	0	4	4		- 6	10	0	10	20	4)	
	5	0	0	5	5		- 5	11	0	10	21	5)	borrow
	6	0	0	6	6		- 4	12	0	10	22	6)	
	7	0	0	7	7		- 3	13	0	10	23	7)	
	8	0	0	8	8		- 2	14	0	10	24	8)	
	9	0	0	9	9		- 1	15	0	10	25	9)	
	10	1	6	16	0)		0	16	1	0	16	0	
	11	1	6	17	1)		1	17	1	0	17	1	
	12	1	6	18	2)		2	18	1	0	18	2	
	13	1	6	19	3)		3	19	1	0	19	3	
	14	1	6	20	4)		4	20	1	0	20	4	
	15	1	6	21	5)	carry	5	21	1	0	21	5	
	16	1	6	22	6)		6	22	1	0	22	6	
	17	1	6	23	7)		7	23	1	0	23	7	
	18	1	6	24	8)		8	24	1	0	24	8	
	19	1	6	25	9)		9	25	1	0	25	9	

TABLE 3

COLUMN

1 Input data and carry bit added to register contents.
Equal to intermediate result (output of processor first part).

2 New CARRY/$\overline{\text{BORROW}}$ bit ("1" = carry).

3 Correction factor.

4 Sum of intermediate result and correction factor

5 Final result (ignoring "16" bit).

6 Input data and borrow bit subtracted from register contents.

7 Intermediate result (output of processor first part).

8 New CARRY/$\overline{\text{BORROW}}$ bit ("0" = borrow).

9 Correction factor.

10 Sum of intermediate result and correction factor.

11 Final result (ignoring "16" bit).

Data Outputs

Three outputs are provided from each board for use as input data. Since digits are processed one at a time, each having ten times the significance of the previous digit, the significance of a data output can be determined by choosing the timing of the digit relative to the clock. Normally the least significant digit is produced in time to be accepted as input data on the first clock pulse of a cycle and so on. In this case the data output has a significance of "1". If the output is taken from a point one

stage later in the shift register, the data will be delayed by one clock pulse (i.e. the least significant digit is produced in time to be accepted on the second clock pulse of a cycle, etc.) and will have a significance of "10". If the digits are advanced by taking from a point earlier on the shift register, the significance of the data is reduced by ten times for each clock pulse advance. The three data outputs provided have significances of "10", "1" and "1/1000".

Input Multiplexer

Each board can select one of 8 sources from which to take its input data. This is performed by a set of four 8-to-1 line multiplexers. The multiplexers have a 3 bit address. The '1' and '2' bits are common to the two boards - separate "4" bits are provided, to allow a certain amount of flexibility in the selection of data sources. The "2" and "4" bits of the multiplexer address are static control wires - the "1" bit is a sequential control wire, although it is only used as such during the "integrate" operation, when its function is to switch the input data source from the "1" digit of the SIN and COS signals to the "10" digit, after the first clock pulse of the cycle. For the allocation of multiplexer addresses, see table 4.

Mpx Address	Register A	Register B
0	SIN 1	COS 1
1	SIN $1\overline{0}$	COS $\overline{10}$
2	10A	10B
3	DATA BUS	DATA BUS
4	LOG. CONST.	B/1000
5	B/1000	A/1000
6	A	B
7	B	A

TABLE 4

Note: The multiplexer address shown here refers to the signals appearing on boards 5 and 6. It should be noted that the "1" bit of the MPX ADDRESS is inverted with respect to the MPX 1 CMD wire originating on board 7.

Strobe Gates

A set of gates is provided to enable none, some, or all of the nine digits of the input data to be added. The "pattern" of digits added to the register is determined by the MPX STROBE wire, a sequential control wire common to both boards. Separate static control wires (STROBE A and STROBE B) are provided, allowing neither, either or both registers to accept input data. When the input data is disabled, zero is added to or subtracted from the register contents, and the multiplexer address is of course irrelevant.

Clear Gates

A set of gates is provided which allows the register contents to be discarded before entering the processor section of the board. These are controlled by the $\overline{\text{CLEAR}}$ wire, a static control wire common to both boards. If this wire is low, the input data is added to or subtracted from zero. This enables the register contents to be cleared or inverted.

Decsh Gates

A set of four AND-OR-INVERT gates is provided so that the data in the register can be made to bypass the processor and the set of four bistables. This means that each digit requires only 8 clock pulses to reach its "home" position. Thus at the end of the cycle each digit has reached one position further, its weight being reduced by a factor of ten. This has the overall effect of shifting the contents of the register down one digit position, dividing its magnitude by ten. The AND-OR-INVERT gates are controlled by the DECSH wire, a static control wire common to both boards. Logic is provided to ensure that the most significant (9th) digit is equal to zero after a Decsh operation (during an integration operation - i.e. while the INT wire is high - the most significant digit will be made equal to 9 after a Decsh operation, if the register contents are negative, as they will be in 10's complement form).

Add Gates

Normally the add/subtract mode of the board is controlled directly by the ADD A CMD (ADD B CMD) wire. However, if both ADD A CMD and ADD B CMD are low, the add/subtract mode is controlled by the sign of the register contents, such that the board will only subtract if the contents are negative. This feature is provided for use by the Complement operation (the only operation for which both ADD A CMD and ADD B CMD are low).

During Integration (i.e. while the INT wire is high) the add/subtract mode is controlled by the SGN SIN (SGN COS) and SGN V wires. An exclusive - OR gate forms the product of these two signals, which then determines the add/subtract mode for the cycle to be performed.

Sign Bistable

Each board is provided with a sign bistable to keep track of the sign of the register contents during add and subtract (and integrate) operations. In order for the bistable to operate correctly, it is necessary for the register contents to be in 10's complement form if negative. The bistable works on the principle that an examination of the sign of the register contents, and whether they are being added or subtracted, will determine whether an operation will change the contents in a direction towards zero or away from it. If the contents will change in a direction away from zero, or if the board is not adding or subtracting, a sign change is impossible, and any change of state of the bistable is inhibited. If the contents of the register will change in a direction towards zero, the new sign can be determined from the ABN CARRY signal (see table 5). Due to propagation delay considerations, the new sign must be computed by a complex set of gates from the data outputs of the first part of the processor, rather than from the ABN CARRY signal. A static control wire which will inhibit changes of the sign bistables regardless of other conditions, is provided (INH. SGN. CH.).

SIGN OF REGISTER CONTENTS	SIGN OF INPUT DATA	ADD/SUBTRACT MODE	SIGN CAN CHANGE	ABN CARRY	NEW SIGN
+	+	ADD	NO	0	-
+	+	SUBTRACT	YES	1	+
+	-	SUBTRACT	NO	0	-
+	-	ADD	YES	1	+
-	-	ADD	NO	0	-
-	-	SUBTRACT	YES	1	+
-	+	SUBTRACT	NO	0	-
-	+	ADD	YES	1	+

TABLE 5

It is assumed that input data in an addition or subtraction operation is coming from the other register. The signal POS B (POS A) indicates whether it is positive or negative. During integration (i.e. when the INT wire is high), this signal is disabled, as the value of SIN (COS) is always regarded as positive (negative values are obtained by subtracting the positive value).

The sign bistables may be loaded from the "1" bit of the data bus if the LOAD, DEC 6 and STROBE A (STROBE B) wires are high, and the $\overline{\text{INH. SGN. CH.}}$ wire is low.

Output Latch

A four bit latch is provided to enable any one of digits 0 to 5 to be latched during a cycle for subsequent reading onto the data bus. It is supplied with a strobe pulse (OUTPUT LATCH STROBE), whose position in the cycle is determined by the DECADE wires, from board 4. The contents of the latch are read onto the data bus if the $\overline{\text{ENABLE A}}$ ($\overline{\text{ENABLE B}}$) and $\overline{\text{DEC 6}}$ $\overline{\text{DEC 7}}$ wires are high. The contents of the sign bistable are read onto the "1" bit of the data bus if the ENABLE A (ENABLE B) and DEC 6 wires are high - they are also available as a separate signal, POS A (POS B), for use by the control logic (via the condition multiplexer).

Dec 9 Zero Gate

An output signal $\overline{\text{DEC 9 A ZERO}}$ ($\overline{\text{DEC 9 B ZERO}}$) is provided to indicate to the control logic (via the condition multiplexer) whether the 9th digit of the register contents is zero.

Delay Bistables

All signals present on the edge - connector of the board are timed so that events associated with the least significant digit occur on the first clock pulse of the cycle, and so on. Static control signals, which affect all 9 digits, change between cycles. However, they may affect various different points on the central loop of the register. The least significant digit may not reach the point affected (the "control point") until one or two clock pulses after the beginning of the cycle, and the most significant digit may not reach it until one or two clock pulses after the beginning of the succeeding cycle, which may not occur for some time after the cycle in question. Bistables are necessary to delay the arrival of control signals until the least significant digit of the register contents arrives at the control point, and to store the signals until the most significant digit has passed this point on the loop.

Bistables in this category are:

1)	Set of 4 input data bistables	(one clock pulse delay)
2)	ADD bistable	(one clock pulse delay)
3)	ADD' bistable	(two clock pulses delay)
4)	INH. SGN. CH bistable	(one clock pulse delay)
5)	CLEAR bistable	(one clock pulse delay)
6)	DECSH bistable	(two clock pulses delay)

Some control signals, while they are static in the sense that their effect is constant for all 9 digits, are not maintained for the whole of the cycle. Bistables which store these signals must not be allowed to change state until the end of the cycle, if the input signal should change. This is achieved by routing the outputs of these bistables back to their inputs for all clock pulses when they are not permitted to change state. The bistables to which this applies are:

1) ADD bistable
2) DECSH bistable
3) POS A (POS B) bistable (slightly different, in that it is the ABN CARRY information that is not maintained, rather than the control signals)

The signal $\overline{\text{CPO}}$ is provided to indicate the first clock pulse of the cycle. A signal indicating the second pulse is generated on the board (CPO'). These signals are used to control changes of state of the bistables shown above, and also to control sections of the board which require a mode change

at some point in the cycle, e.g.:

1) Carry and borrow must be inhibited for the first digit.
2) Decsh gates must force the 9th digit to zero or nine.

Logic Convention

All data inputs and outputs to the board are in negative logic. However, some parts of the board (principally the processor and the set of 4 bistables) operate in positive logic. These are indicated in fig. 3.

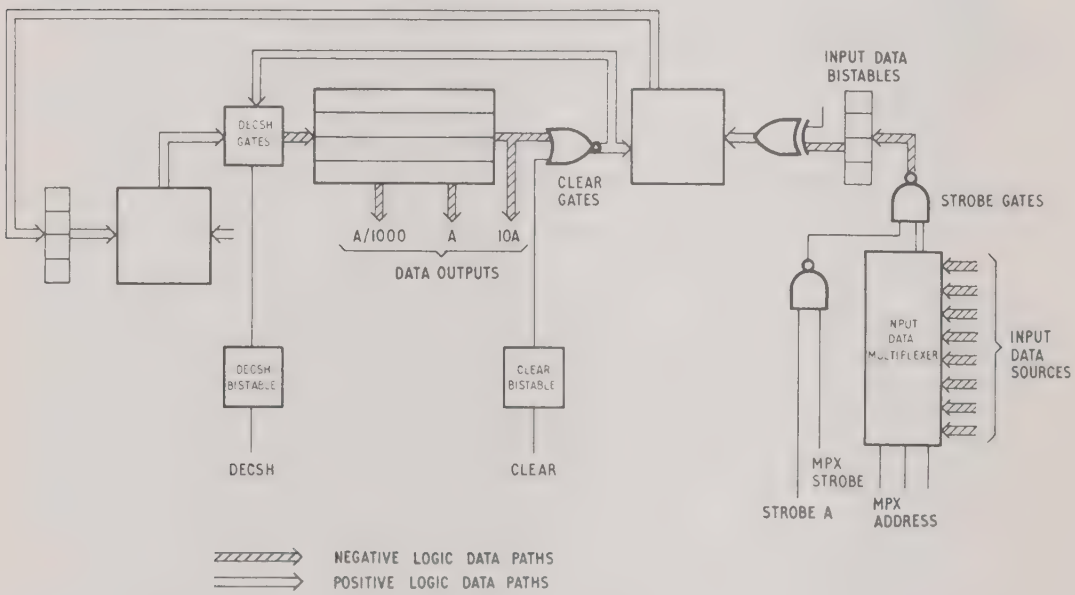


Fig. 3 Logic Data Paths.

INTRODUCTION TO SEQUENCE LOGIC

The "sequence logic" is situated on board 4. Its function is to interlock the arithmetic unit and control logic timing, and to produce all clocks and sequential signals required by the arithmetic unit. The operation of the sequence logic will be described for all operations except for integration, in this chapter.

The sequence logic can be subdivided into the following sections.

1. Clock generator
2. Sequential control signal generator
3. Clock enable logic
4. Sequence control

1. Clock Generator

The clock input to the board is a continuous 10MHz clock. A continuous 5MHz clock is derived from this by a bistable operating as a divide by 2 stage. The 5MHz clock drives most of the bistables in the sequence logic.

The $\overline{\text{PRECLOCK}}$ signal is also generated by this section of the board. This signal is used as a clock by the arithmetic register boards (5 and 6). It is a train of pulses, occurring in groups of 9, at a rate of 5MHz. The pulses within a single arithmetic unit operation are continuous, but the number of pulses is always a multiple of 9. Incomplete cycles are not allowed. An 8 bit shift register is used to ensure that pulses occur in groups of 9. The shift register is clocked by the $\overline{\text{PRECLOCK}}$ signal. Its input (named $\overline{\text{CPO}}$) is high if any one of its stages is set to "0". If all the 8 stages are set to "1", the input ($\overline{\text{CPO}}$), which will become the state of the first stage after the next clock pulse, is low. There are thus 9 states through which the shift register can pass:-

STAGE	1	2	3	4	5	6	7	8	Input (CPO)
	1	1	1	1	1	1	1	1	0
	0	1	1	1	1	1	1	1	1
	1	0	1	1	1	1	1	1	1
	1	1	0	1	1	1	1	1	1
	1	1	1	0	1	1	1	1	1
	1	1	1	1	0	1	1	1	1
	1	1	1	1	1	0	1	1	1
	1	1	1	1	1	1	0	1	1
	1	1	1	1	1	1	1	0	1

The $\overline{\text{PRECLOCK}}$ signal is generated by a bistable clocked by the 10MHz clock. The output of this bistable follows the 5MHz clock if either the $\overline{\text{CPO}}$ signal or the CLOCK ENABLE signal is high. If both these signals are low, the output of the PRECLOCK bistables is permanently high (i.e. the clock stops). This means that the clock can only stop with the shift register in the first state shown above, which occurs once every 9 pulses. The number of clock pulses which occur in a group must be a multiple of 9. The CLOCK ENABLE signal is used to initiate or maintain a group of clock pulses. If the signal is removed the clock will stop when the next multiple of 9 is reached. A signal (C in P) indicating that a cycle is in progress, is produced for use by the "sequence control" section.

2. Sequential Control Signal Generator

A number of "sequential control signals" are produced whose state depends upon the stage in the cycle which has been reached. These signals are used by other parts of the arithmetic unit. They are generated from the outputs of the shift register and the position of the "0" in the shift register, if any, indicates which of the 9 clock pulses has been reached.

The signals are (See Fig. 1):

	SIGNAL	USED BY BOARDS
1.	$\overline{\text{CPO}}$	5,6
2.	ITERATION CLOCK	7,8
3.	MPX STROBE	5,6
4.	OUTPUT LATCH STROBE	5,6
5.	MPX ADDR 1	5,6
6.	LOG CONST. $\overline{8}$	5
7.	LOG CONST. $\overline{4}$	5
8.	LOG CONST. $\overline{2}$	5
9.	LOG CONST. $\overline{1}$	5

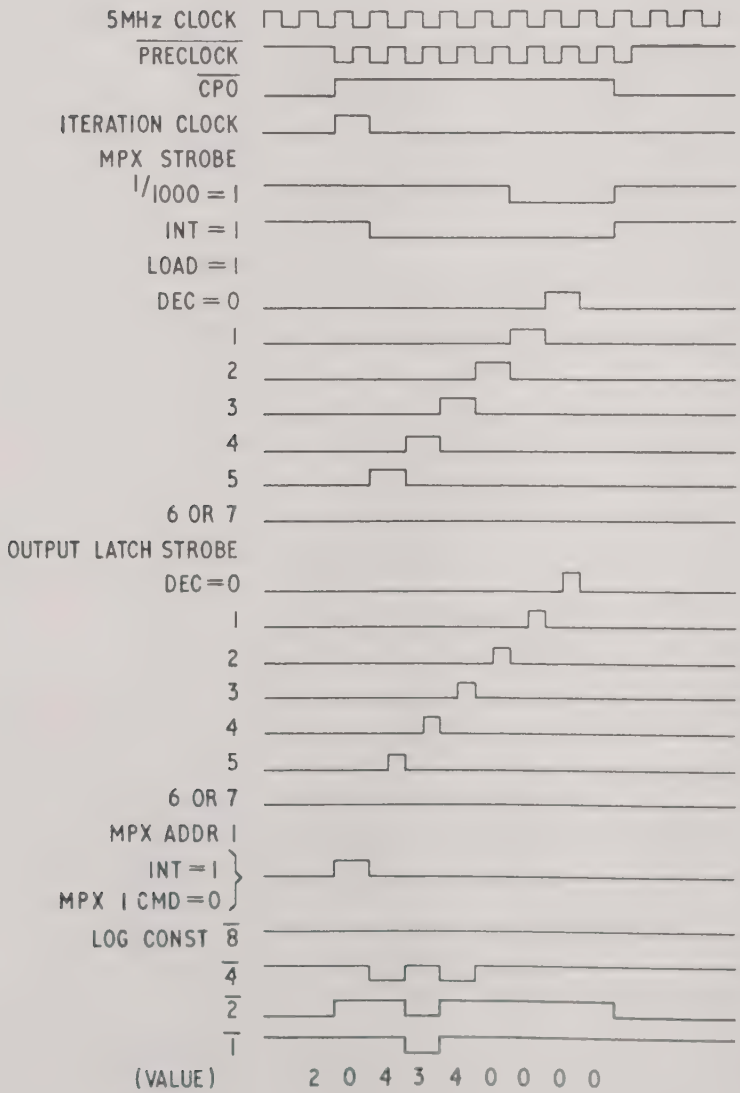


Fig. 1 Arithmetic Unit Timing Diagram.

3. Clock Enable Logic

This section is composed of gates only. Its function is to initiate an arithmetic unit operation, and to terminate it when the appropriate conditions are satisfied. It has a number of modes of operation, which are selected by the STOP CODE A and STOP CODE B wires.

a) Single cycle operations. (See Fig. 2).
STOP CODE A = high
STOP CODE B = high
Nine clock pulses are produced in this mode. The CLOCK ENABLE wire remains high for one clock pulse (200nSec) only to initiate a cycle,. and the operation finishes at the end of the cycle.

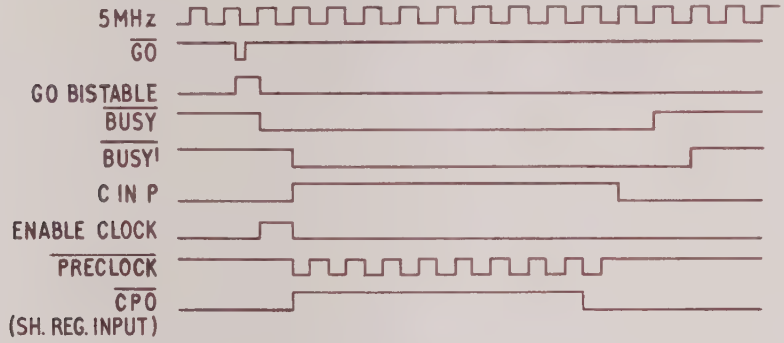


Fig. 2 Single Cycle Operation

b) Iterative operations. (See Fig. 3).
i) STOP CODE A = high
STOP CODE B = low

In this mode cycles continue until either the TIMER/ITERATION OFLO wire goes low or the ABN CARRY A wire goes high. When either of these things happens, the CLOCK ENABLE wire goes low, and the clock stops at the end of the cycle. Since the clock can only finish at one point in the cycle, the state of the ABN CARRY A wire is irrelevant except between the last clock pulse of one cycle and the first clock pulse of the next (the level of this signal may in fact change at any or all clock pulses). Change of state of the TIMER/ITERATION OFLO signal should occur slightly after the 2nd clock pulse of the cycle (i.e. slightly after the iteration clock edge).

If the TIMER/ITERATION OFLO signal is low when an operation is requested, no cycles will be performed. The ABN CARRY signal however is ignored for the first cycle (this signal may have been left high by the previous operation) - if ITERATION/TIMER OFLO is high before the operation, at least one cycle must occur.

ii) STOP CODE A = low
STOP CODE B = high

In this mode the conditions which must be satisfied to terminate the operation are the same as (i) above, except:-
ABN CARRY B is used in place of ABN CARRY A
Both ABN CARRY B and TIMER/ITERATION OFLO are ignored for the first cycle. In this mode, at least one cycle must occur.
In both (i) and (ii) above, the TIMER/ITERATION OFLO signal is assumed to be present if DECADE number 6 or 7 is selected. In this case the operation will stop after no cycles (case (i)) or one cycle (case (ii)) respectively. This is a precaution only, to prevent infinitely long operations when the wrong DECADE is selected.

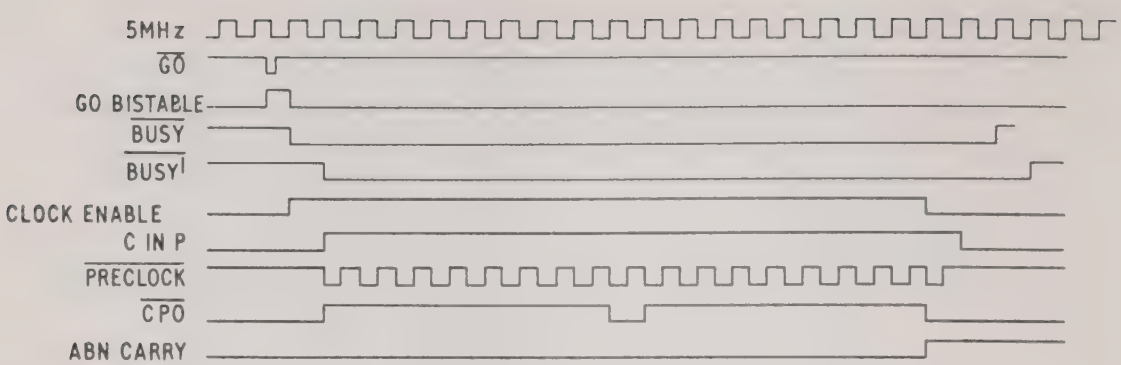


Fig. 3(a) Iterative Operation (Stopped By ABN CARRY).

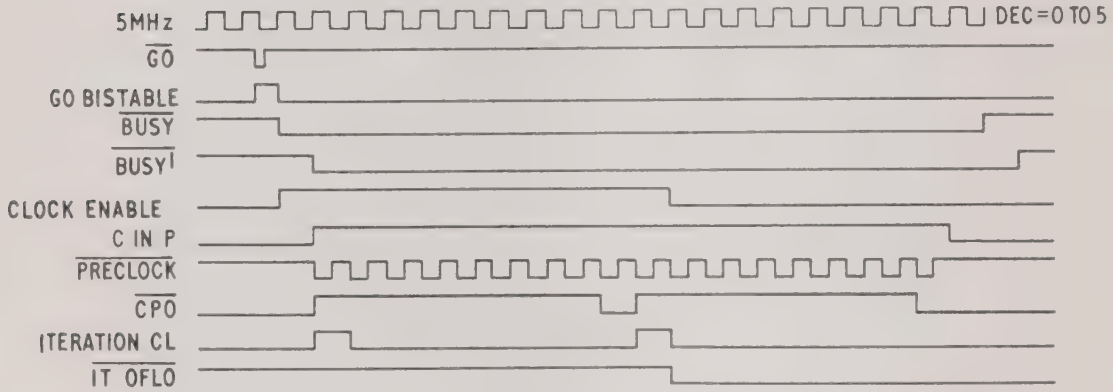


Fig. 3(b) Iterative Operation (Stopped By IT OFLO).

c) STOP CODE A = low
STOP CODE B = low

This mode is never used.

4. Sequence Control

This section consists of a number of bistables and gates. Its function is to accept the command to perform an operation (the $\overline{GO}$ pulse) from the control logic, generate the BUSY signal which indicates to the control logic that an arithmetic unit operation is in progress, and to instruct the clock enable logic to initiate the operation.

The $\overline{GO}$ pulse is accepted by an RS bistable and stored until the next 5MHz clock pulse. The BUSY bistable is then set (a maximum of 200nS after the leading edge of the GO pulse), which causes the $\overline{BUSY}$ signal to the control logic to go low, inhibiting further control logic action. The RS bistable is reset at this point, provided that the $\overline{GO}$ pulse has finished (otherwise it will remain set until GO pulse finishes). A BUSY' bistable follows the BUSY bistable with 1 clock pulse (200nSec) delay. The BUSY' signal is used to enable most of the conditions for terminating operations (the $\overline{TIMER\ ITERATION\ OFLO}$ signal is permanently enabled if STOP CODE B = low, causing no cycles to be performed under certain conditions - see 3, b, i above). Initially BUSY = low and BUSY' = low. The termination conditions are thus disabled. When BUSY goes high, the CLOCK ENABLE wire will go high, (except in the special case mentioned in 3, b, i above) and the operation will commence. On the next clock pulse, BUSY' will go high, enabling the termination conditions. The operation will continue until these conditions are met.

The BUSY bistable remains set as long as the C in P bistable is set. When the operation is finished, the C in P bistable will reset, and the following clock pulse, the BUSY bistable will reset, allowing the $\overline{\text{BUSY}}$ wire to the control logic to go high. The control logic will then procede to the next instruction, and the arithmetic unit will remain quiescent until the next $\overline{\text{GO}}$ pulse. The BUSY bistable cannot reset if CLOCK ENABLE is high. This prevents it from resetting at the beginning of an operation, before the C in P bistable is set.

INTRODUCTION TO THE CONTROL LOGIC

The arithmetic unit is only capable of performing simple operations autonomously. Each stage in the calculation of the results or in the calculation of the new frequency in a frequency sweep, involves many such steps. Other parts of the instrument also require commands at various points in the measuring sequence (see Table A). It is the function of the control logic to issue these commands in the correct sequence to perform whatever action is requested by the touch keys. In fact the instrument is performing a continuous sequence of operations whenever it is switched on, as the state of waiting for a command from the front panel involves a sequence of examining in turn each touch key from which a command could come.

Sections requiring commands from control logic.	Nature of commands
1. Arithmetic unit	32 arithmetic operations, including data transfers to and from the store.
2. Store	Read and write commands in conjunction with the arithmetic unit (see above)
3. Keyboard display	Update local display data buffer from the appropriate store location.
4. Keyboard	a. Disable keyboard while the machine is running b. Switch SINGLE button to OFF at the end of the measurement. c. Switch sweep button to OFF at the end of a frequency sweep, or if the synchroniser (1185) is in use.
5. Autorange counter	a. The counter used to control the input range in the autorange sequence is set to the 10mV range at the beginning of the sequence. b. Increment autorange counter.
6. Input system	Various modes may be selected: a. Measure bias b. Reject bias
7. Peripherals	The machine indicates to any peripherals that may be attached (plotter, teletype, computer etc.) that the results are ready to be accepted.

Table A Control Logic Functions

The control logic follows a program of 1024 instructions. Each of these is an 8 bit word, - they are stored in four 2048 bit read-only memory IC's (Board 11, IC's 19, 24, 32, 39). The program includes jump instructions, sub-routines and conditional instructions. An instruction may be internal to the control logic (e.g. a jump instruction, or an instruction setting an internal memory bistable), or may involve one or more other sections of the machine. Conditional instructions are used so that changes in the state of other sections of the instrument may affect the path taken by the control logic through the program. The control logic can monitor the state of various counters and bistables within itself in the same way (see Table B).

ARITHMETIC UNIT CONDITIONS

Group	No.	Name	Source	Meaning
2	0	$\overline{\text{DEC 9 ZERO A}}$	Register A (Board 5)	Is the 9th decade of register A equal to zero?
2	1	$\overline{\text{DEC 9 ZERO B}}$	Register B (Board 6)	Is the 9th decade of register B equal to zero?
2	2	EXP C POS	Exponent counter (Board 7)	Is EXP C positive? (i.e. EXP B ≥ EXP A)
2	3	$\overline{\text{EXP C ZERO}}$	Exponent counter (Board 7)	Is EXP C equal to zero? (i.e. EXP B = EXP A)
2	4	POS A	Register A (Board 5)	Are the contents of register A positive?
2	5	POS B	Register B (Board 6)	Are the contents of register B positive?
2	11	ARITH BS 1	Board 7	Is bistable no.1 set?
2	12	ARITH BS 2	Board 7	Is bistable no.2 set?

TOUCH KEY CONDITIONS

Group	No.	Name	Source	Meaning
1 1	4 5	Measure mode X Measure mode Y	Touch keys Touch keys	Which of keys X, Y, Y/X is selected?
1 1	11 12	Measure sequence SINGLE Measure sequence RECYCLE	Touch keys Touch keys	Which of keys STOP, SINGLE, RECYCLE is selected?
1 1	10 9	Sweep ON Sweep DOWN/ HOLD	Touch keys Touch keys	Which of keys OFF, HOLD, UP, DOWN is selected?
1	13	Sweep LOG	Touch keys	Which of keys LIN LOG is selected?
1	15	ENTER FREQUENCY	Touch keys	Has the ENTER key been pressed? (with FREQUENCY selected)
1	14	ENTER VOLTS	Touch keys	Has the ENTER key been pressed? (with OUTPUT VOLTS selected)
1	3	REJECT BIAS	Touch keys	Is the REJECT BIAS key selected?

TABLE B

INTERNAL CONDITIONS

Group	No.	Name	Source	Meaning
2	7	INPUT X/$\overline{Y}$	Input channel bistable	Are the input channel relays set to X or Y?
2	13	$\overline{\text{MEASURE BIAS}}$	Measure bias bistable	Is "measure bias" mode selected?
1	2	MARKER BISTABLE	Marker bistable	Is the bistable set? (local memory element)
1	8	SWEEP BISTABLE	Sweep bistable	Is the bistable set? (i.e. is this the first measurement of a frequency sweep)?
1	6	ARITH DEC 8	Arithmetic decade counter	Is the 8 bit of the counter set?

MISCELLANEOUS EXTERNAL CONDITIONS

Group	No.	Name	Source	Meaning
1	0	INPUT RELAY FLAG	Input relays	Are the relays in the process of changing?
1	1	AUTORANGE OVERLOAD	Autorange logic (Board 17)	Has integration been terminated by an overload during an autorange measurement?
2	10	OVERLOAD	Autorange logic (Board 17)	Has overload occurred during this measurement?
2	14	PERIPHERAL FLAG	Peripherals	Have all peripherals which may be attached to the instrument finished receiving the results, or programming the instrument?
2	9	SYNCHRONISER FLAG	Synchroniser (1185) option	Is the measurement value of the period of the synchronising signal ready for processing?
2	8	$\overline{\text{LEAD}}$/LAG	Lead/lag link (Board 7)	Is the instrument set to measure lead angles (link present) or lag angles (link absent)?
2	6	Input system settling delay	Delay Monostable (Board 7)	Is the delay monostable set? This allows a 30mS period for the input system to settle after altering the range during an autorange sequence.
1	7	STORE OVERLOAD	Store	Is the overload bit set in the currently addressed store word?
2	15	SPARE FLAG		

In order to control the states of other sections of the instrument, various pulse and level outputs are available (see Table D).

PULSE OUTPUT	DESTINATION	FUNCTION
$\overline{GO}$	Arithmetic unit	Initiate instruction specified by INSTRUCTION CODE lines.
RESET RANGE	Autorange counter	Reset range to 10mV at beginning of autorange sequence.
INC. RANGE	Autorange counter	Increment range during autorange sequence.
$\overline{CHANGE\ FREQ}$	a) Keyboard display b) Peripherals	Update local display data buffer from frequency or volts location in store. Indicates that results are ready to be output.
MOS STORE WRITE	Store	Write current data bus digit into store.
RESET OVERLOAD	Autorange logic	Reset overload bistable at beginning of measurement.
$\overline{CMD\ DELAY}$	Delay monostable (Board 7)	Initiate input system settling delay (used after changing range in auto-range sequence).
$\overline{RESET\ SWEEP}$	Touch keys	Reset sweep buttons to OFF.

LEVEL OUTPUT	DESTINATION	FUNCTION
INSTRUCTION CODE	Arithmetic unit	5 lines - select one of 32 arithmetic unit operations. 1 line - enable programmable arithmetic unit bistables.
DECADE NO.	Arithmetic unit	Select one of 8 decades.
MEASURE BIAS	Arithmetic unit Input system	Select "measure bias" mode.
X/$\overline{Y}$ RELAYS	Input channel relays	Select channel X or Y
COMPUTE	a) RUN lamp b) Peripherals	RUN lamp is on when $\overline{COMPUTE}$ = 0 Control data sourcing and data receiving peripherals.
RUN	Touch keys	Disable keyboard while RUN = 0 Switch SINGLE button off at end of measurement.
ENABLE A, $\overline{B}$, C,	Arithmetic unit	Enable arithmetic unit register A, B or C to write data onto the arithmetic unit data bus.

Table D Control Logic Output Signals

1.3 Circuit Diagrams

Most of the circuit diagrams have been laid out with groups of components which perform certain functions confined within imaginary blocks. The corners of the blocks are included in the drawing. The purpose of the blocks is to assist the reader to follow the functional paths throughout the system.

Some diagrams, notably those in the digital section, are not functionally divided. This is due to the nature of the signals within these boards making the functional tracing of signal paths a practical impossibility. Fault finding on these boards (pcb 2 - 5, 7, 8, 10 - 13 and 15 - 17) should only be attempted with the aid of special test equipment.

Immediately following this introduction is a chart showing the relation between these circuit diagrams and the printed circuit boards. The purpose of this chart is to provide the link between the functional circuit diagrams and the physical location of the components. It also indicates the major functional areas of the instrument.

List of Circuit Diagrams

1	1172 Osc/Mixer	39	1172 Touch Key Latches (2)
2	1170 Clock Dividers	40	1172 Touch Key Latches (3)
3	1170 Buffer Dividers	41	1172 Touch Key Latches (4)
4	1170 Ramp Control	42	1170 Power Input
5	1172 Ramp Gen.	43	1170 Earthy P.S.
8	1172 Reversible Counter Cont.	44	1170 Floating P.S.
9	1172 Reversible Counter	45	1170 Sensing Amp.
10	1172 Shaper	46	Power Dist. (+5V)
11	1172 Main Modulator	47	Power Dist. (+18V & 16V)
12	1172 Voltage Control	48	Power Dist. (11V & 0V)
13	1172 Attenuator	50	1170 PCB No. 2 (Complete)
14	1172 Main Output	52	1170 PCB No. 3 (1)
15	1172 Bias Modulator	53	1170 PCB No. 3 (2)
16	1172 Bias Output	54	1170 PCB No. 4 (Complete)
17	1172 Floating P.S.	55	1170 PCB No. 5 (Complete)
18	1172 Floating Dist.	56	1170 PCB No. 7 (Complete)
19	1172 Input Relays	57	1170 PCB No. 8 (Complete)
20	1170 Input Circuit	58	1170 PCB No. 10 (1)
21	1170 Demod; & V to F	59	1170 PCB No. 10 (2)
22	1170 Bias Input Gen.	60	1170 PCB No. 10 (3)
23	1170 Bias Input Control	61	1170 PCB No. 10 (4)
24	1170 Bias Input Ranging	62	1170 PCB No. 11 (1)
25	1172 Strobe Gen.	63	1170 PCB No. 11 (2)
26	Touch Keys (1)	64	1170 PCB No. 11 (3)
27	Touch Keys (2)	65	1170 PCB No. 11 (4)
28	Touch Keys (3)	66	1170 PCB No. 12 (1)
29	1172 Serialiser	67	1170 PCB No. 12 (2)
30	1172 Pulse Shaper	68	1170 PCB No. 12 (3)
31	1170 Latch Store Control	69	1170 PCB No. 13 (Complete)
32	1170 Latch Store (1)	70	1170 PCB No. 15 (Complete)
33	1170 Latch Store (2)	71	1170 PCB No. 16 (Complete)
34	1170 Latch Store (3)	72	1170 PCB No. 17 (1)
35	1170 Latch Store (4)	73	1170 PCB No. 17 (2)
36	1170 Latch Store (5)	74	Display Assy (1)
37	Latch Store Output	75	Display Assy (2)
38	1172 Touch Key Latches (1)		

CIRCUIT DIAGRAMS

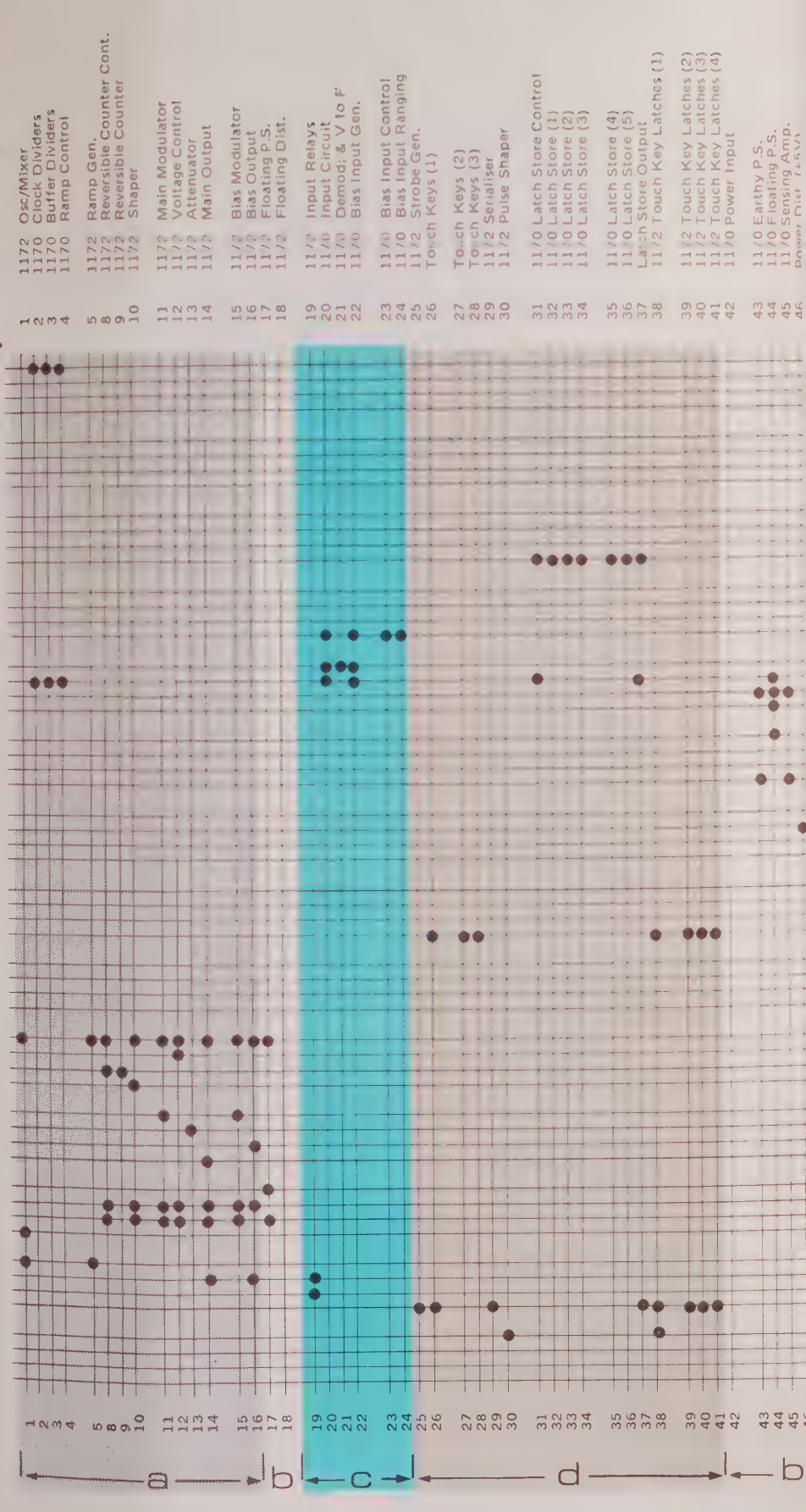
PRINTED CIRCUIT BOARDS

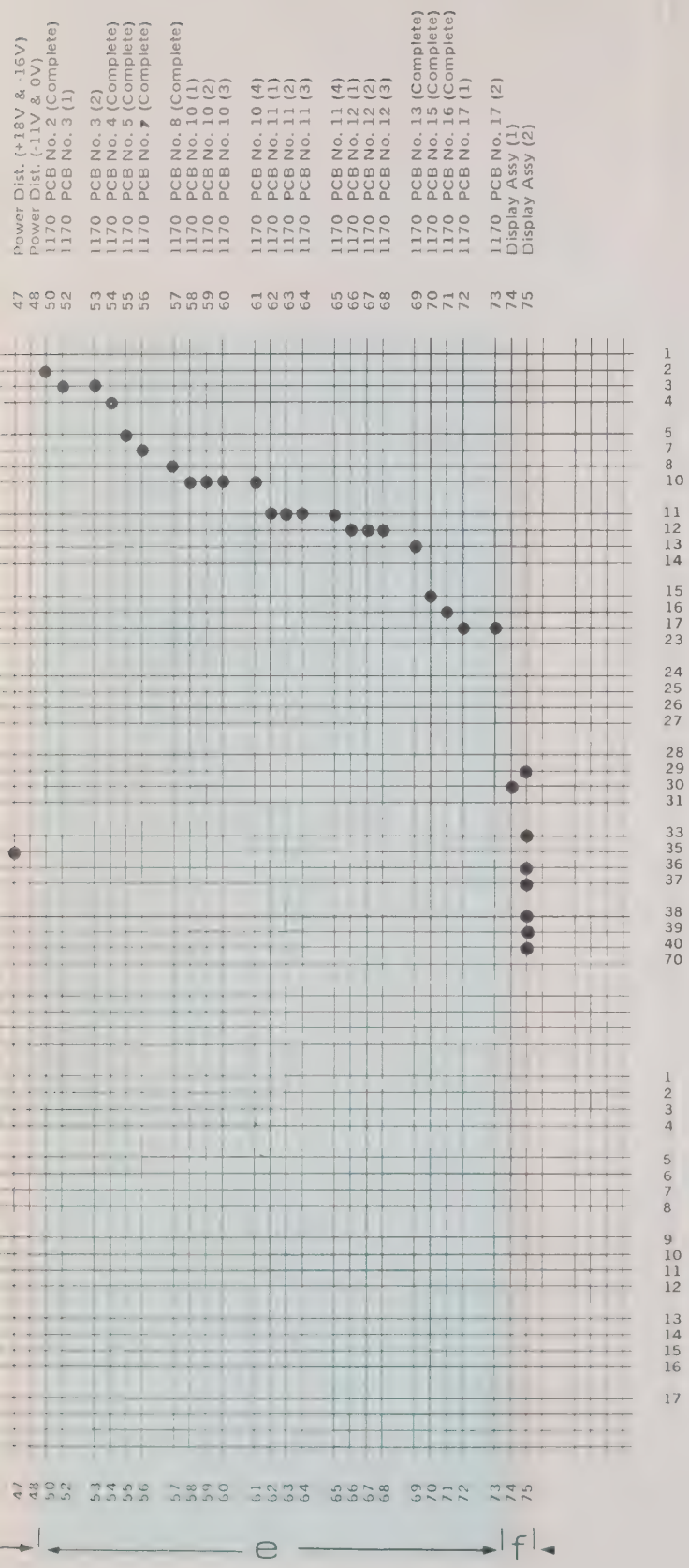
1170

Synthesiser Divider	1
N Cycle/Gen Divider	2
SIN/COS Gen.	3
Arith. Control Seq. Logic	4
Arith. Reg. A	5
Exp. Counter & Decode	7
Iteration Counter	8
Main Control A	10
Main Control B	11
Main Store	12
Equiv. Gates	13
Latch Store	14
Keyboard Control	15
Exp. Keyboard Control	16
Autorange Dig. D/A	17
Input Bias	23
Input Amp.	24
Mother Board	25
Power Supply	26
Rectifier Board	27
Rectifier Board	28
Display Power Supply	29
Display	30
P.S. Protection	31
Neon Board A	33
Capacitor Board	35
Neon Board B	36
Neon Board C	37
Neon Board D	38
Neon Board E	39
Neon Board F	40
Front Panel Touch Control (Fitted to the 1172)	70

1172

Mother Board	1
D/A Converter	2
Reversible Counter	3
Sine Shaping	4
Signal Conditioning	5
Prog. Attenuator	6
Bias O/P Amplifier	7
O/P Amplifier	8
Power Supply	9
Interface	10
Interface Driver	11
Osc. Mixer	12
Phase Detector	13
Relay Switches	14
Relay Timing	15
Front Panel Control	16
Front Panel Relay	17





This chart shows the relation between the printed circuit boards and the circuit diagrams of the 1170 series.

The board numbers are repeated on the right-hand side of the chart for convenience and likewise the circuit numbers at the bottom of the chart.

The main purpose of the chart is to allow easy cross-reference between the circuit diagrams in Section 1 of the Servicing Manual and the pcb information in Section 2.

The spots indicate which numbers of circuit diagrams should be consulted for each pcb. For instance, the chart shows that the circuit diagram of board 10 of the 1170 will be found on circuits No. 58 to 61.

It should be noted that as far as the circuits are concerned the 1172 and 1177 are identical, except that certain parts of the 1172 are not included on the 1177.

The major functional areas of the instrument are shown by the following key.

a Generator

b Power Supplies

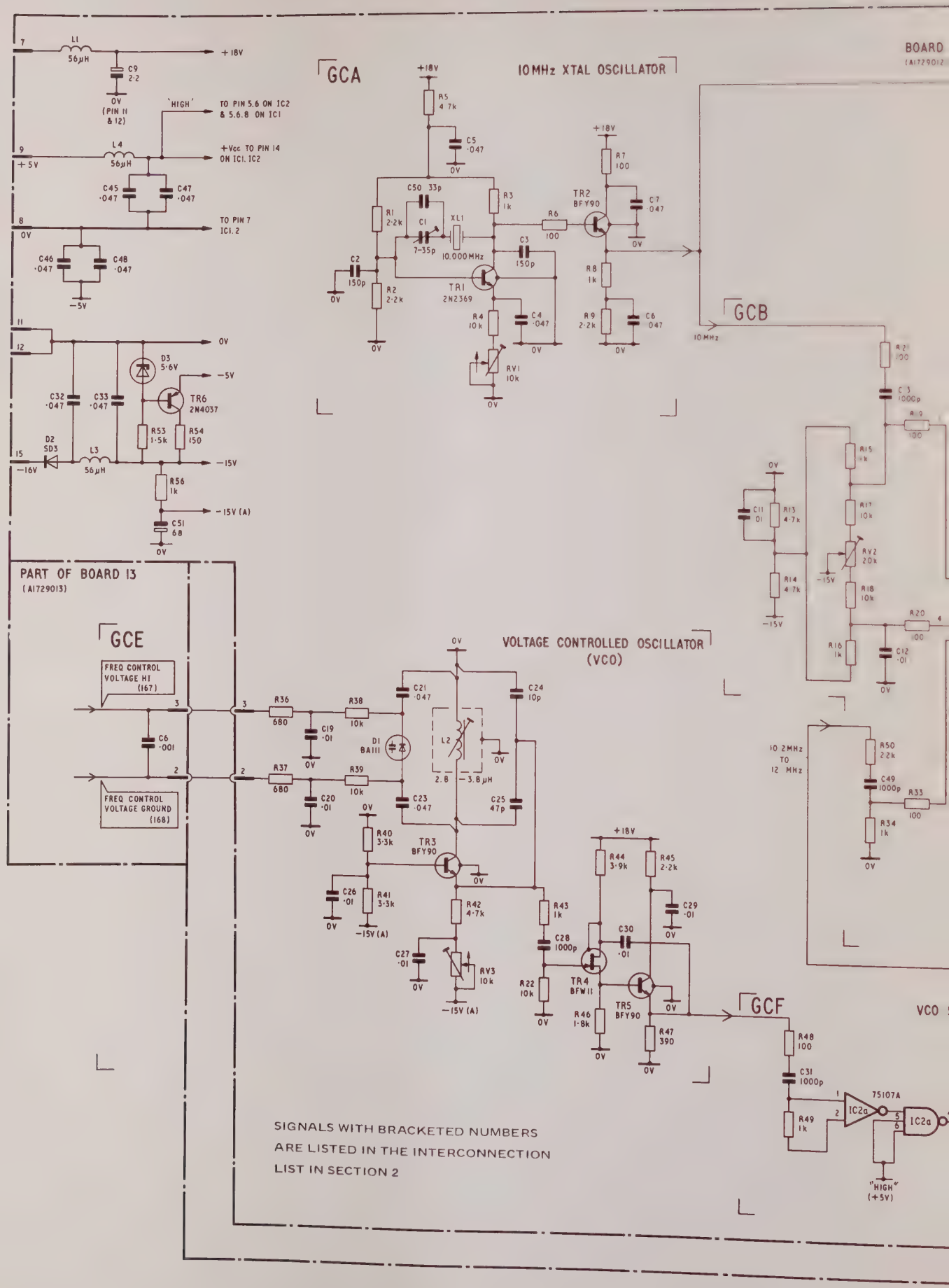
c Input System

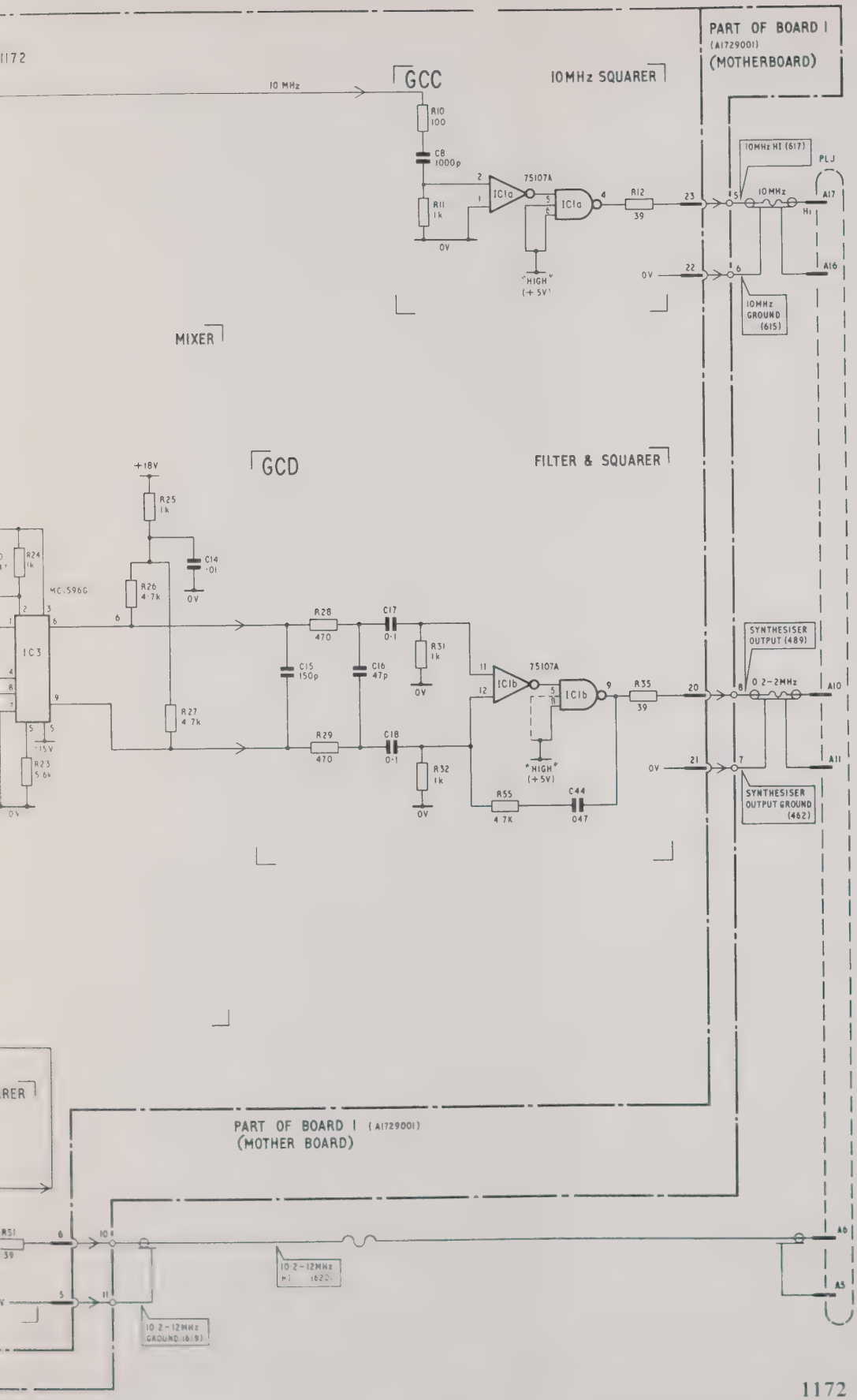
d Selector Latching

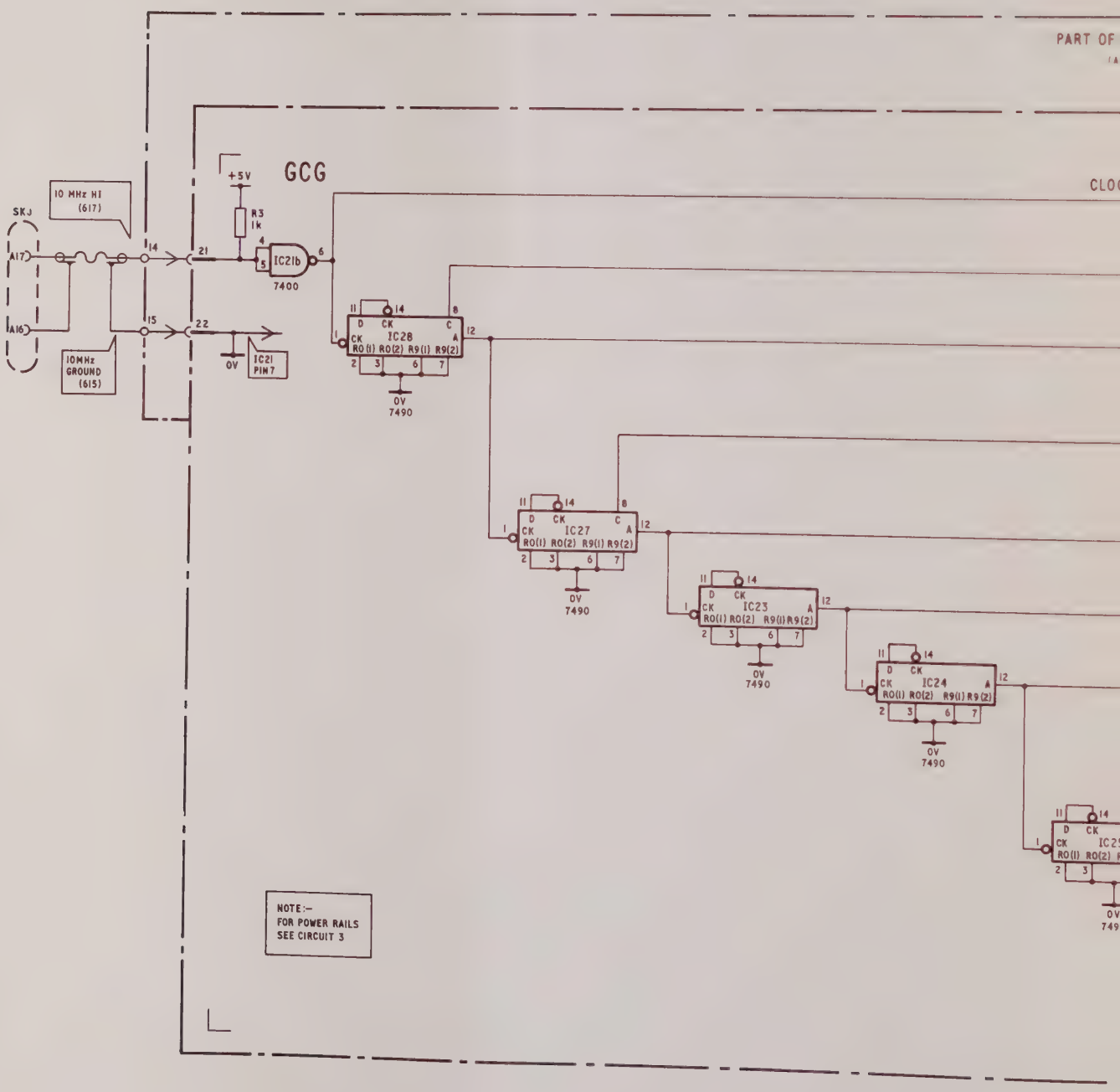
e Digital Section

f Display

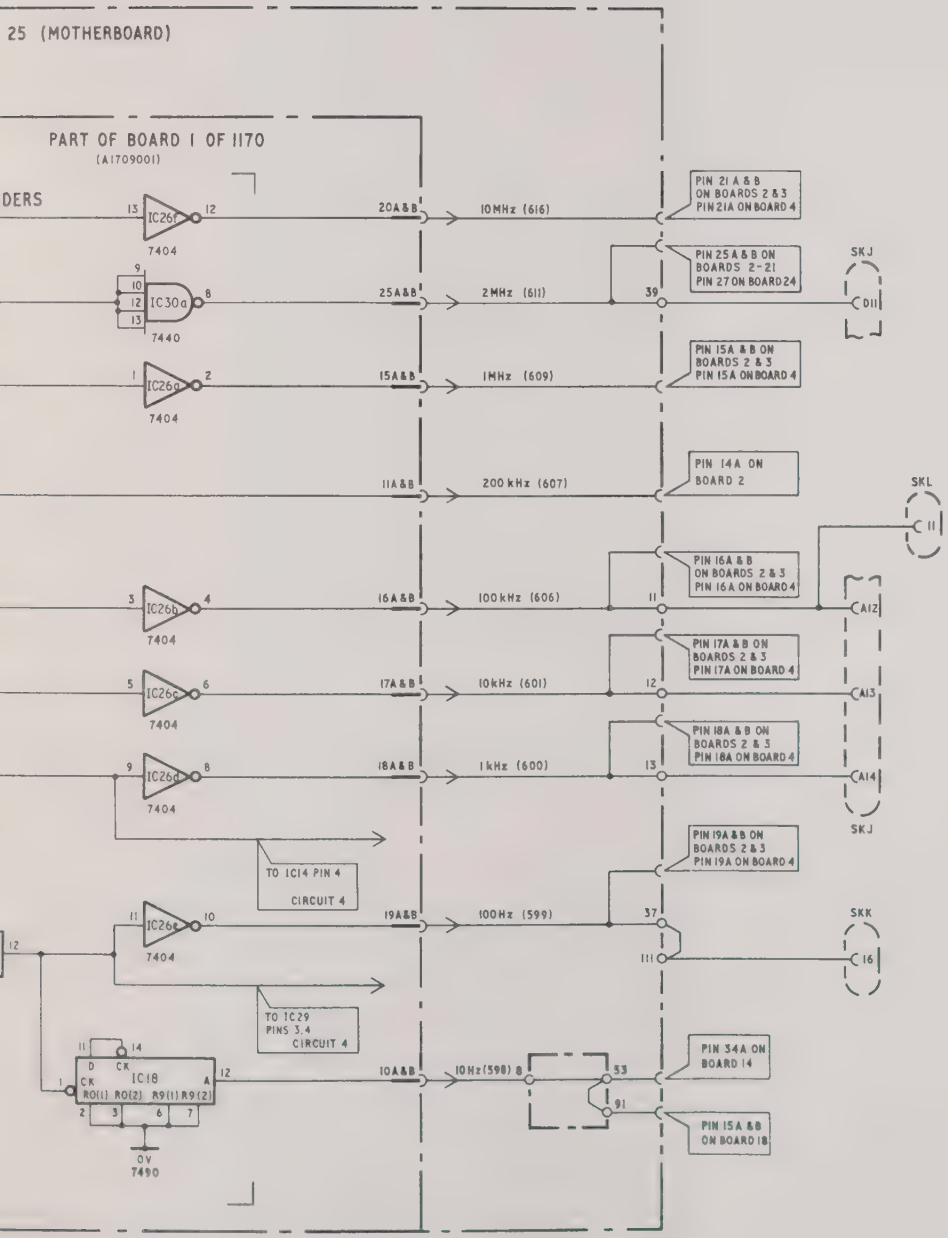
ALLOCATION CHART

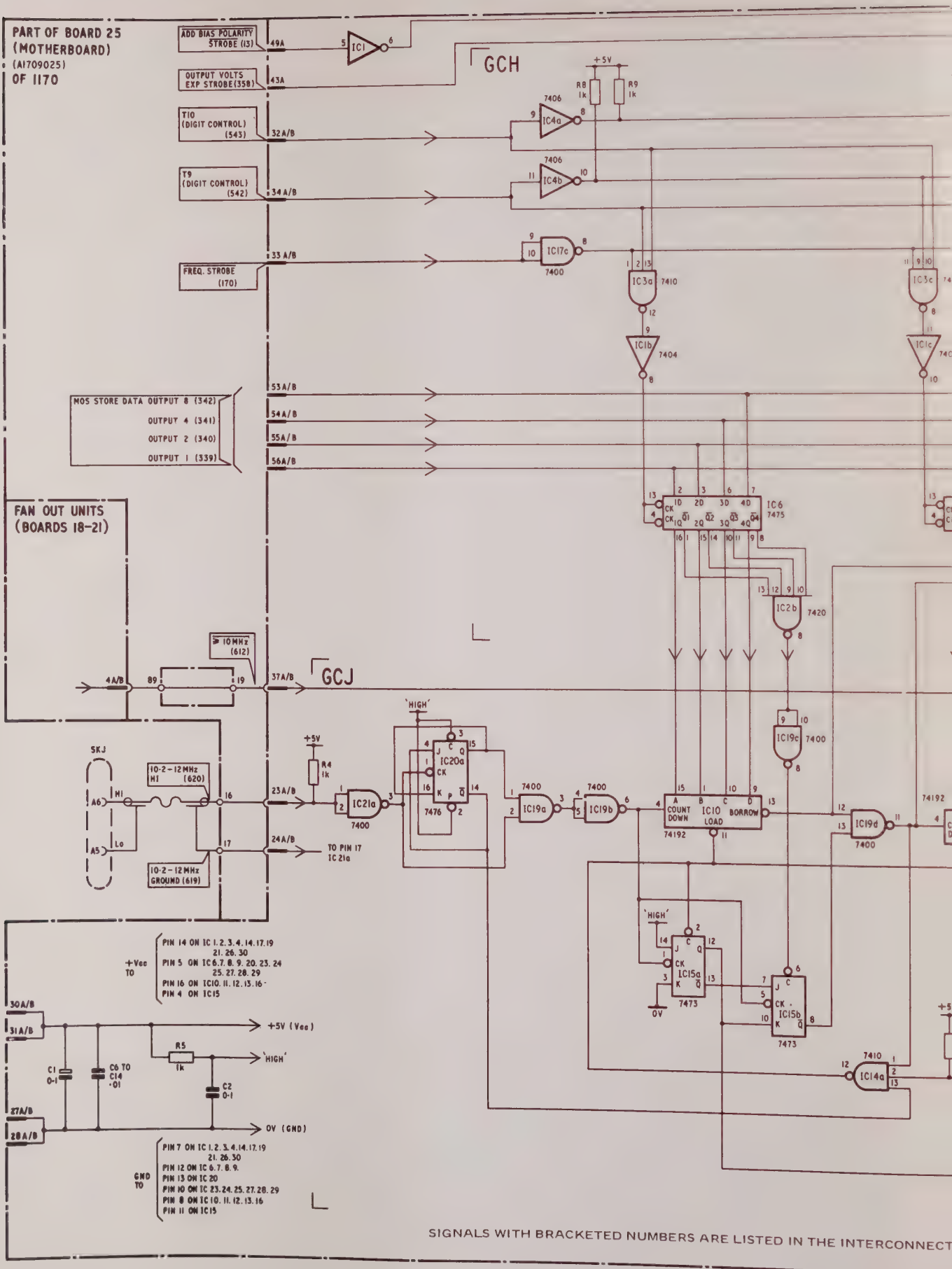

BOARD
(AI729012
GCA
10MHz XTAL OSCILLATOR
+18V
R5 4·7k
C5 ·047
0V
R7 100
C7 ·047
C50 33p
R3 1k
TR2 BFY90
R1 2·2k
C1 7-35p
XL1
10.000MHz
R6 100
C3 150p
C2 150p
R2 2·2k
TR1 2N2369
R8 1k
R4 10k
C4 ·047
R9 2·2k
C6 ·047
RV1 10k
10MHz
GCB
L1 56µH
C9 2·2
+18V
'HIGH'
TO PIN 5.6 ON IC2 & 5.6.8 ON IC1
+Vcc TO PIN 14 ON IC1, IC2
+5V
L4 56µH
C45 ·047
C47 ·047
TO PIN 7 IC1, 2
C46 ·047
C48 ·047
−5V
D3 5·6V
−5V
C32 ·047
C33 ·047
TR6 2N4037
R53 1·5k
R54 150
D2 SD3
L3 56µH
−16V
−15V
R56 1k
−15V (A)
C51 68
PART OF BOARD 13
(AI729013)
GCE
FREQ CONTROL VOLTAGE HI (167)
FREQ CONTROL VOLTAGE GROUND (168)
C6 ·001
R36 680
R37 680
R38 10k
R39 10k
C19 ·01
C20 ·01
C21 ·047
C23 ·047
C24 10p
C25 47p
D1 BA111
L2
2·8 − 3·8µH
VOLTAGE CONTROLLED OSCILLATOR (VCO)
R40 3·3k
TR3 BFY90
C26 ·01
R41 3·3k
−15V (A)
R42 4·7k
C27 ·01
RV3 10k
R43 1k
C28 1000p
R22 10k
TR4 BFW11
TR5 BFY90
R44 3·9k
R45 2·2k
C29 ·01
C30 ·01
R46 1·8k
R47 390
GCF
R48 100
C31 1000p
R49 1k
75107A
IC2a
IC2a
"HIGH" (+5V)
R21 100
C 1000p
R15 1k
R17 10k
RV2 20k
R18 10k
R16 1k
C11 ·01
R13 4·7k
R14 4·7k
−15V
R20 100
C12 ·01
10·2MHz TO 12·1MHz
R50 22k
C49 1000p
R33 100
R34 1k
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

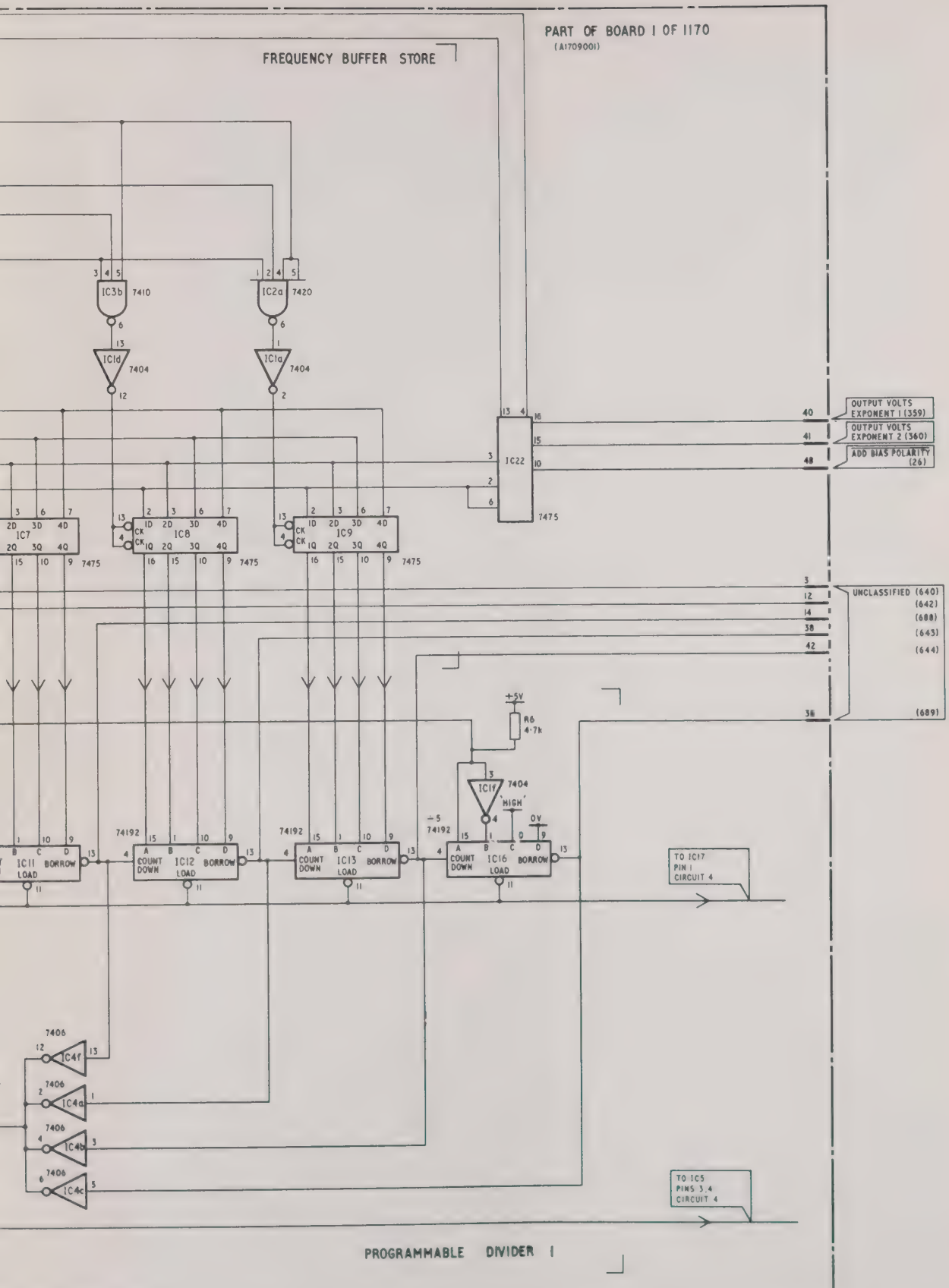

1172
10 MHz
GCC
10MHz SQUARER
PART OF BOARD I
(A1729001)
(MOTHERBOARD)
R10
100
C8
1000p
R11
1k
0V
75107A
IC1a
IC1a
R12
39
"HIGH"
(+5V)
10MHz HI (617)
PLJ
10MHz
A17
Hi
A16
0V
10MHz
GROUND
(615)
MIXER
GCD
FILTER & SQUARER
+18V
R25
1k
C14
·01
0V
R24
1k
MC.596G
IC3
R26
4·7k
R27
4·7k
-15V
R23
5·6k
R28
470
C17
0·1
R31
1k
C15
150p
C16
47p
R29
470
C18
0·1
R32
1k
IC1b
IC1b
75107A
R35
39
"HIGH"
(+5V)
R55
4·7K
C44
·047
SYNTHESISER
OUTPUT (489)
0·2-2MHz
A10
A11
SYNTHESISER
OUTPUT GROUND
(462)
PART OF BOARD I (A1729001)
(MOTHER BOARD)
A6
A5
10·2-12MHz
10·2-12MHz
GROUND (619)



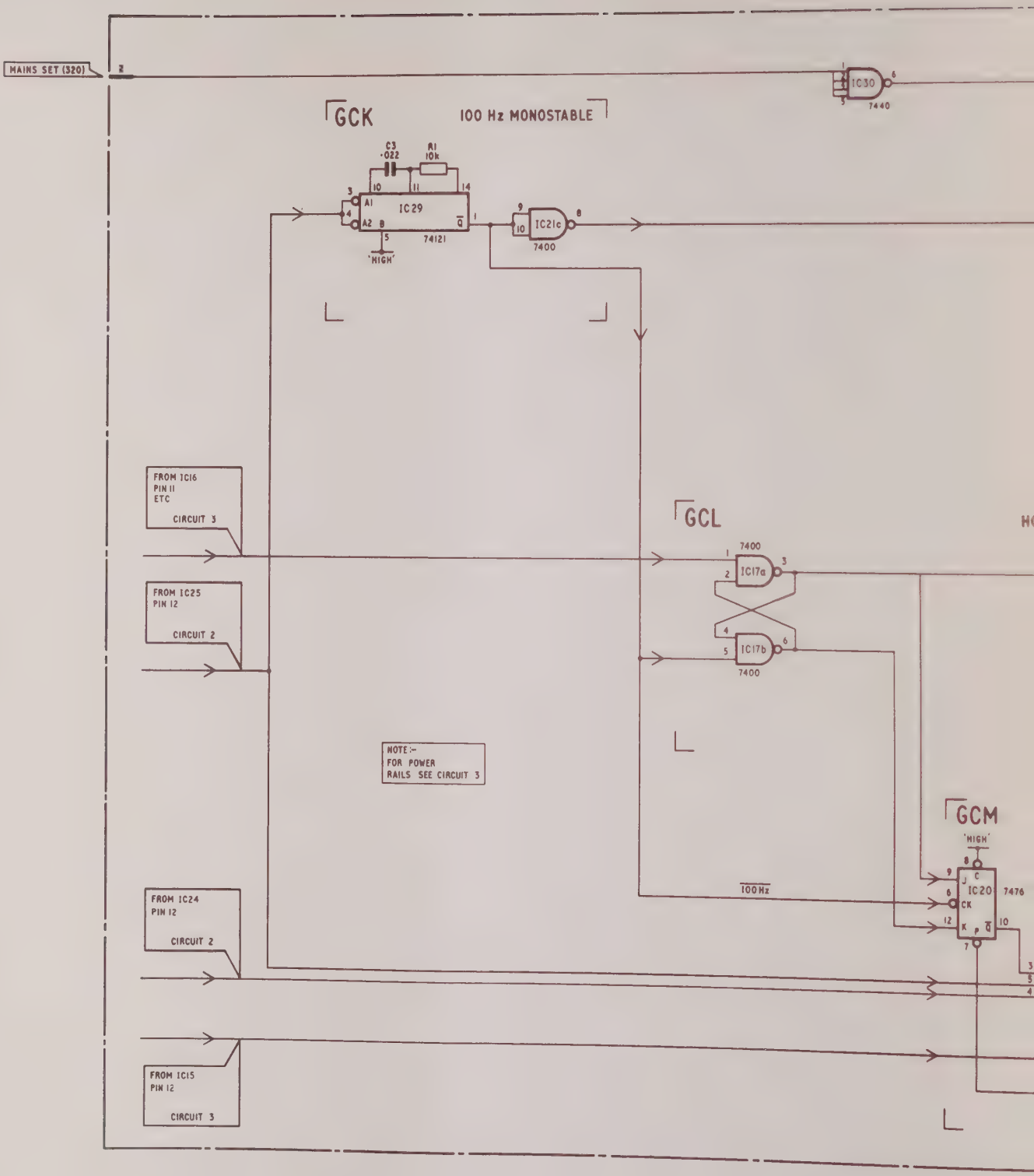
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


25 (MOTHERBOARD)
PART OF BOARD 1 OF 1170
(A1709001)
DERS
IC26f
7404
IC30a
7440
IC26g
IC26b
IC26c
IC26d
IC26e
IC18
7490
20A&B
10MHz (616)
25A&B
2MHz (611)
15A&B
1MHz (609)
11A&B
200kHz (607)
16A&B
100kHz (606)
17A&B
10kHz (601)
18A&B
1kHz (600)
19A&B
100Hz (599)
10A&B
10Hz(598)
PIN 21 A & B ON BOARDS 2 & 3 PIN 21A ON BOARD 4
PIN 25A & B ON BOARDS 2-21 PIN 27 ON BOARD 24
PIN 15A & B ON BOARDS 2 & 3 PIN 15A ON BOARD 4
PIN 14A ON BOARD 2
PIN 16A & B ON BOARDS 2 & 3 PIN 16A ON BOARD 4
PIN 17A & B ON BOARDS 2 & 3 PIN 17A ON BOARD 4
PIN 18A & B ON BOARDS 2 & 3 PIN 18A ON BOARD 4
PIN 19A & B ON BOARDS 2 & 3 PIN 19A ON BOARD 4
PIN 34A ON BOARD 14
PIN 15A & B ON BOARD 18
SKJ
SKL
SKK
TO IC14 PIN 4 CIRCUIT 4
TO IC29 PINS 3,4 CIRCUIT 4

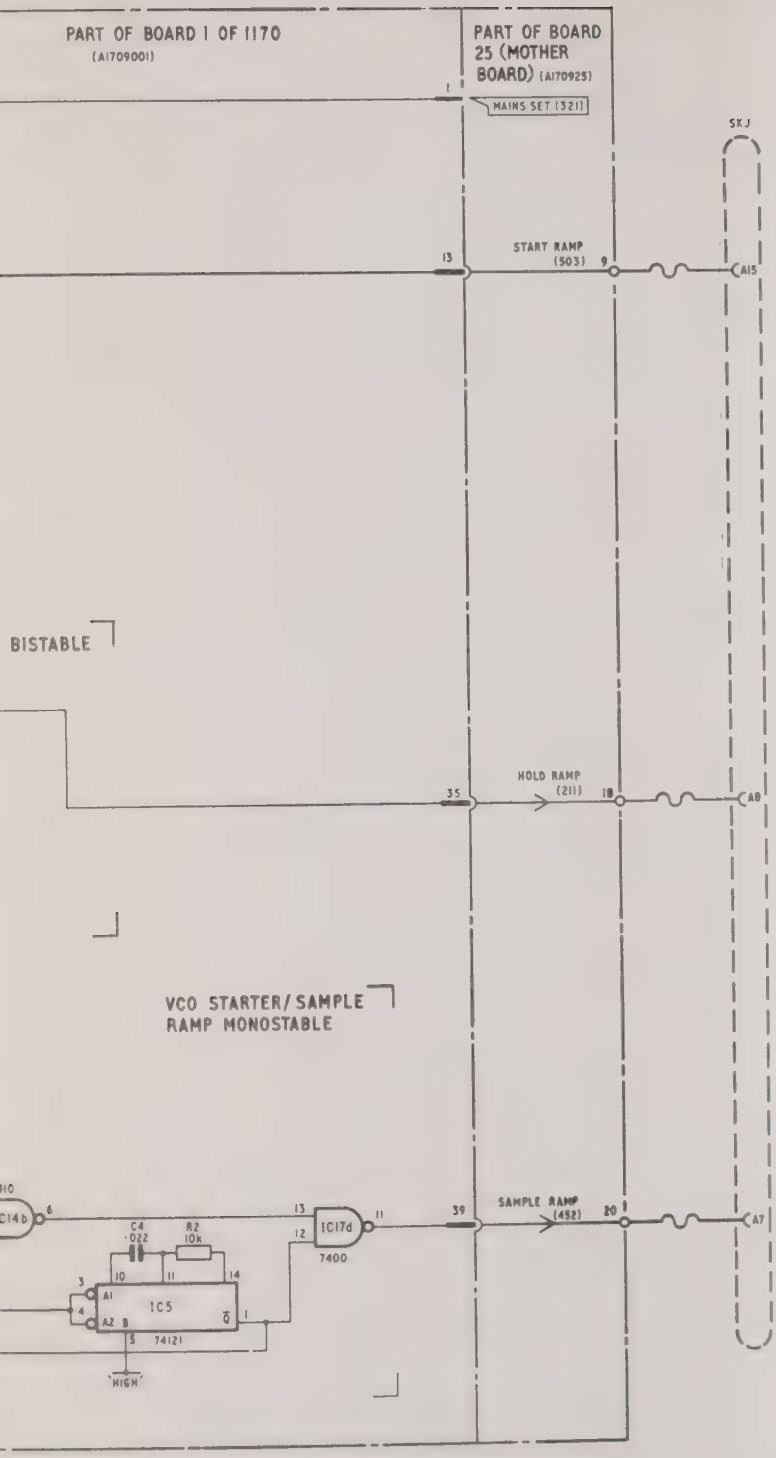

PART OF BOARD 25
(MOTHERBOARD)
(A1709025)
OF 1170
ADD BIAS POLARITY STROBE (13)
OUTPUT VOLTS EXP STROBE (358)
T10 (DIGIT CONTROL) (543)
T9 (DIGIT CONTROL) (542)
FREQ. STROBE (170)
MOS STORE DATA OUTPUT 8 (342)
OUTPUT 4 (341)
OUTPUT 2 (340)
OUTPUT 1 (339)
FAN OUT UNITS
(BOARDS 18-21)
GCH
GCJ
49A
43A
32A/B
34A/B
33A/B
53A/B
54A/B
55A/B
56A/B
4A/B
37A/B
23A/B
24A/B
TO PIN 17 IC 21a
IC1
IC4a
IC4b
IC17c
IC3a
IC3c
IC1b
IC1c
IC6
IC2b
IC20a
IC21a
IC19a
IC19b
IC19c
IC19d
IC10
IC15a
IC15b
IC14a
IC2a
7406
7400
7410
7404
7475
7420
7476
7473
74192
+5V
R8 1k
R9 1k
R4 1k
R5 1k
'HIGH'
0V
SKJ
HI
Lo
A6
A5
10-2-12 MHz HI (620)
10-2-12 MHz GROUND (619)
≥ 10 MHz (612)
+Vcc TO
PIN 14 ON IC 1. 2. 3. 4. 14. 17. 19 21. 26. 30
PIN 5 ON IC 6. 7. 8. 9. 20. 23. 24 25. 27. 28. 29
PIN 16 ON IC 10. 11. 12. 13. 16
PIN 4 ON IC 15
GND TO
PIN 7 ON IC 1. 2. 3. 4. 14. 17. 19 21. 26. 30
PIN 12 ON IC 6. 7. 8. 9.
PIN 13 ON IC 20
PIN 10 ON IC 23. 24. 25. 27. 28. 29
PIN 8 ON IC 10. 11. 12. 13. 16
PIN 11 ON IC 15
30A/B
31A/B
27A/B
28A/B
+5V (Vcc)
'HIGH'
0V (GND)
C1 0-1
C6 TO C14 .01
C2 0-1
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECT

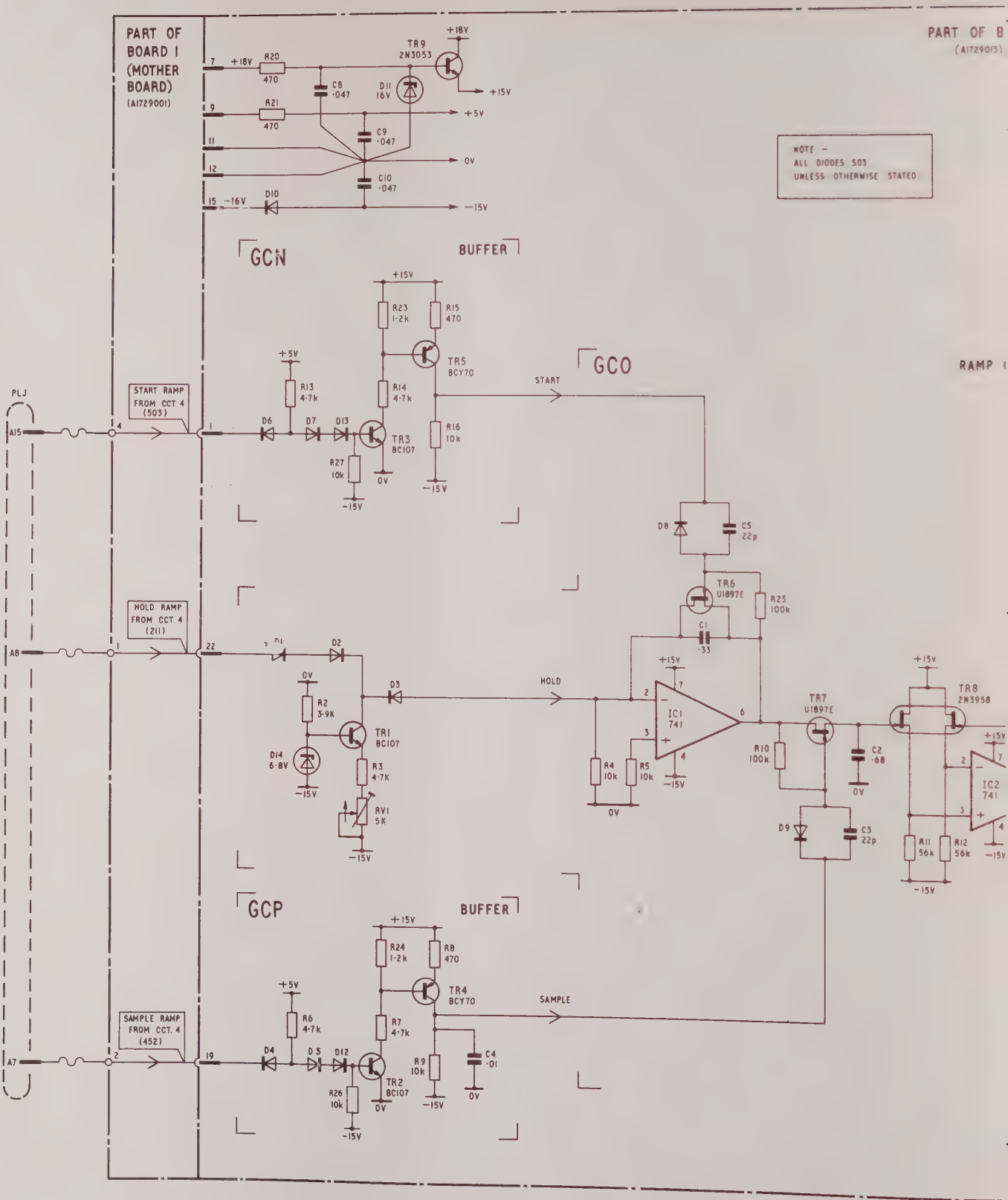


ON LIST IN SECTION 2



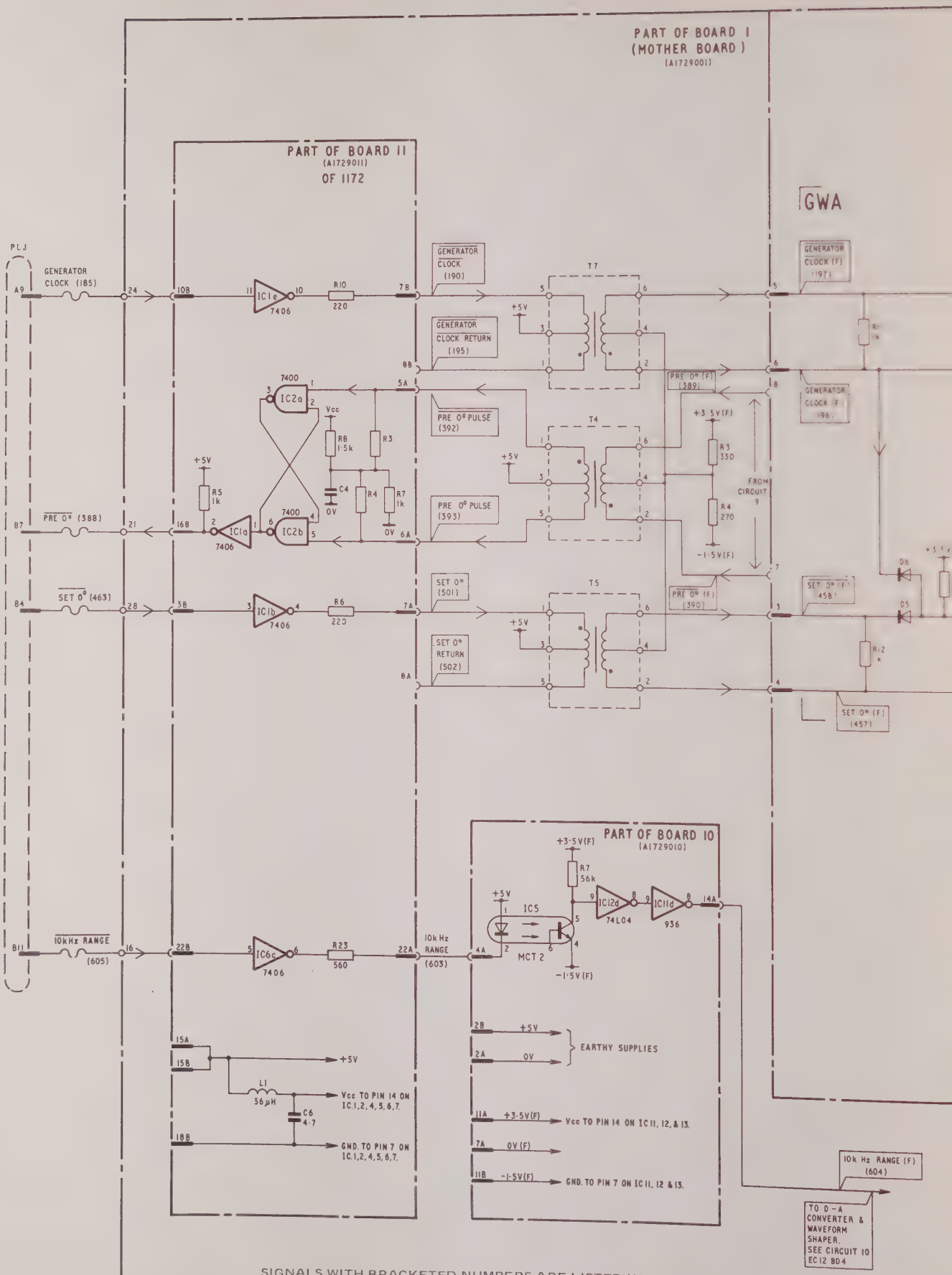
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


PART OF BOARD 1 OF 1170
(A1709001)
PART OF BOARD 25 (MOTHER BOARD) (A170925)
MAINS SET (321)
SKJ
START RAMP (503)
A15
BISTABLE
HOLD RAMP (211)
A8
VCO STARTER/SAMPLE RAMP MONOSTABLE
SAMPLE RAMP (452)
A7
C4 ·022
R2 10k
1C17d
7400
1C5
74121
HIGH



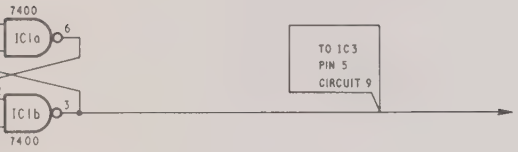
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

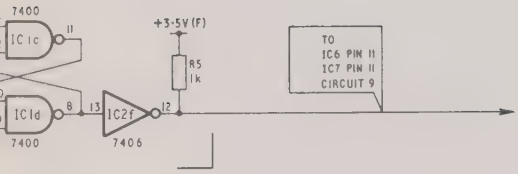
OARD 13 OF 1172
GENERATOR
6
FREQ CONTROL
VOLTAGE HI (167) CIRCUIT 1
FREQ CONTROL
VOLTAGE GROUND (168)
0V


PART OF BOARD I
(MOTHER BOARD)
(A1729001)
PART OF BOARD II
(A1729011)
OF 1172
GWA
PLJ
GENERATOR CLOCK (185)
A9
24
10B
IC1e
7406
R10
220
7B
GENERATOR CLOCK (190)
T7
GENERATOR CLOCK RETURN (195)
8B
5A
PRE 0° PULSE (392)
T4
PRE 0° PULSE (393)
6A
B7
PRE 0° (388)
21
16B
IC1a
IC2b
IC2a
7400
7406
R5 1k
R8 1·5k
R3
R4
R7 1k
C4
0V
Vcc
+5V
B4
SET 0° (463)
28
3B
IC1b
R6
220
7A
SET 0° (501)
SET 0° RETURN (502)
8A
B11
10kHz RANGE (605)
16
22B
IC6c
R23
560
22A
10k Hz RANGE (603)
PART OF BOARD 10
(A1729010)
+3·5V(F)
R7 56k
IC5
MCT 2
IC12d
74L04
IC11d
936
14A
4A
−1·5V(F)
15A
15B
18B
L1 56µH
C6 4·7
+5V
Vcc TO PIN 14 ON IC 1, 2, 4, 5, 6, 7.
GND. TO PIN 7 ON IC 1, 2, 4, 5, 6, 7.
2B
2A
EARTHY SUPPLIES
11A
Vcc TO PIN 14 ON IC 11, 12, & 13.
7A
0V (F)
11B
GND. TO PIN 7 ON IC 11, 12 & 13.
GENERATOR CLOCK (F) (197)
GENERATOR CLOCK F (196)
PRE 0° (F) (389)
+3·5V(F)
R3 330
R4 270
FROM CIRCUIT 9
−1·5V(F)
PRE 0° (F) (390)
SET 0° (F) (458)
SET 0° (F) (457)
D6
D5
10k Hz RANGE (F) (604)
TO D-A CONVERTER & WAVEFORM SHAPER. SEE CIRCUIT 10 EC12 BD4
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

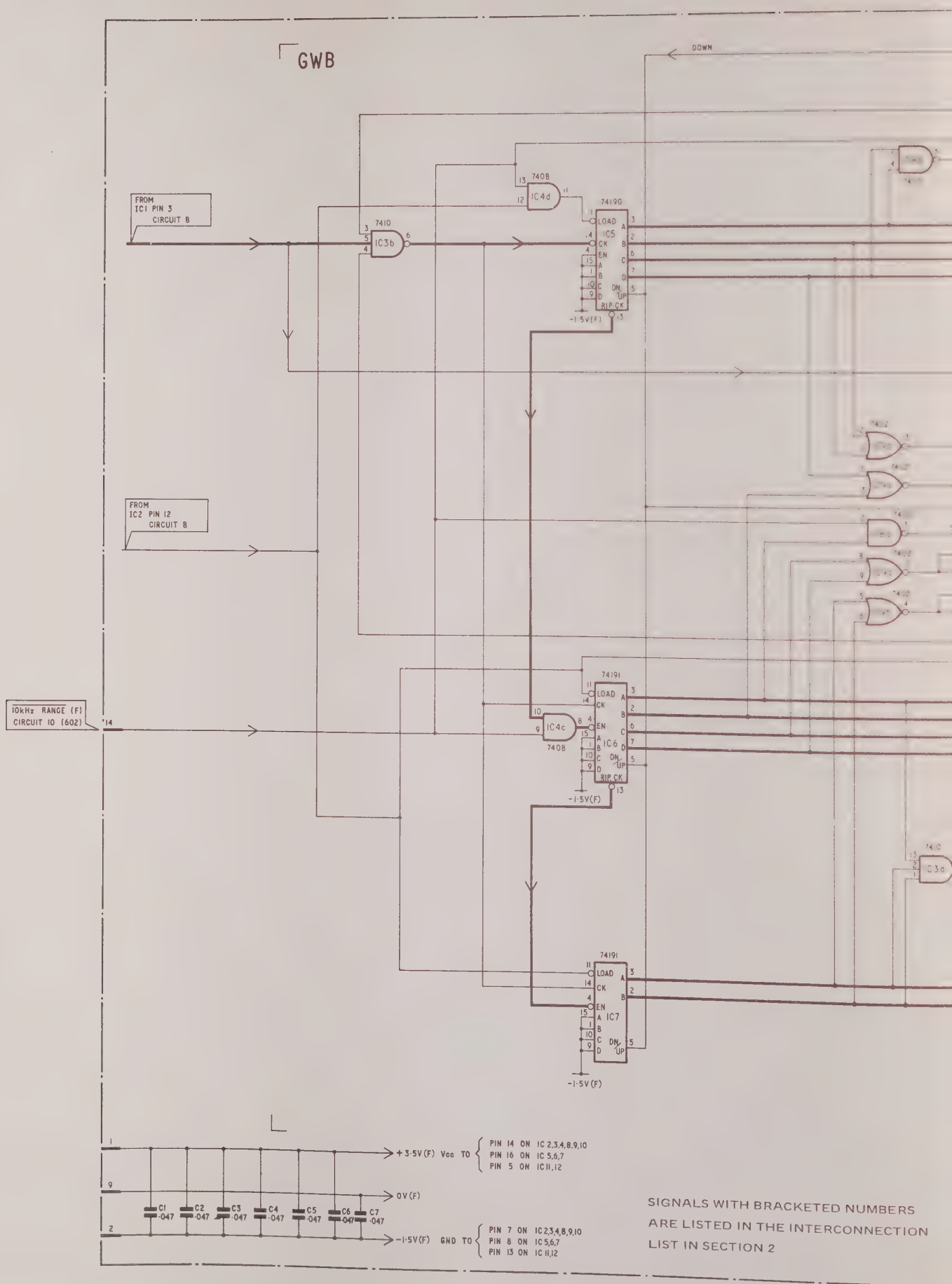
PART OF BOARD 3 OF 1172
(A1729003)

STEP CONTROL

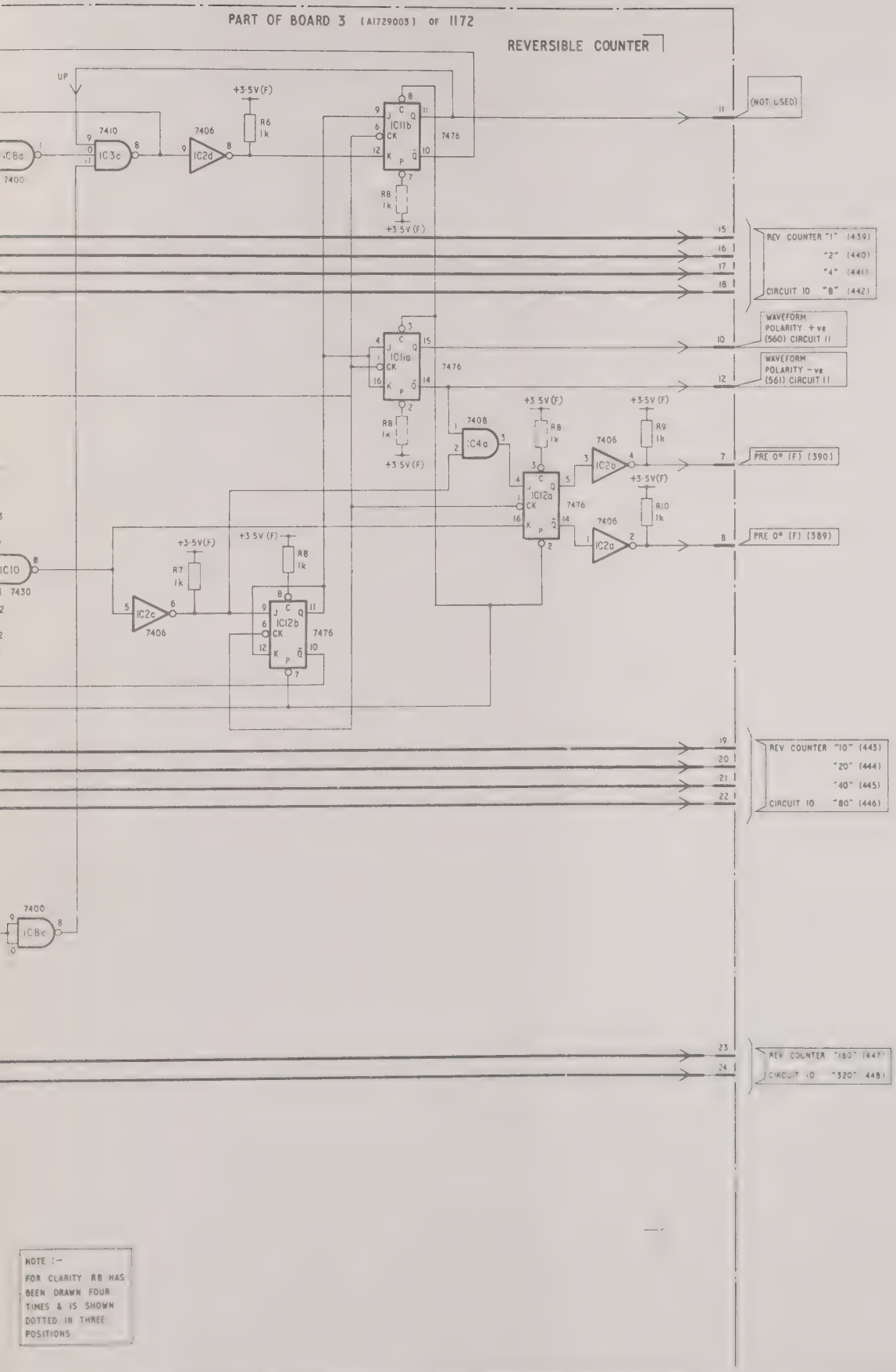


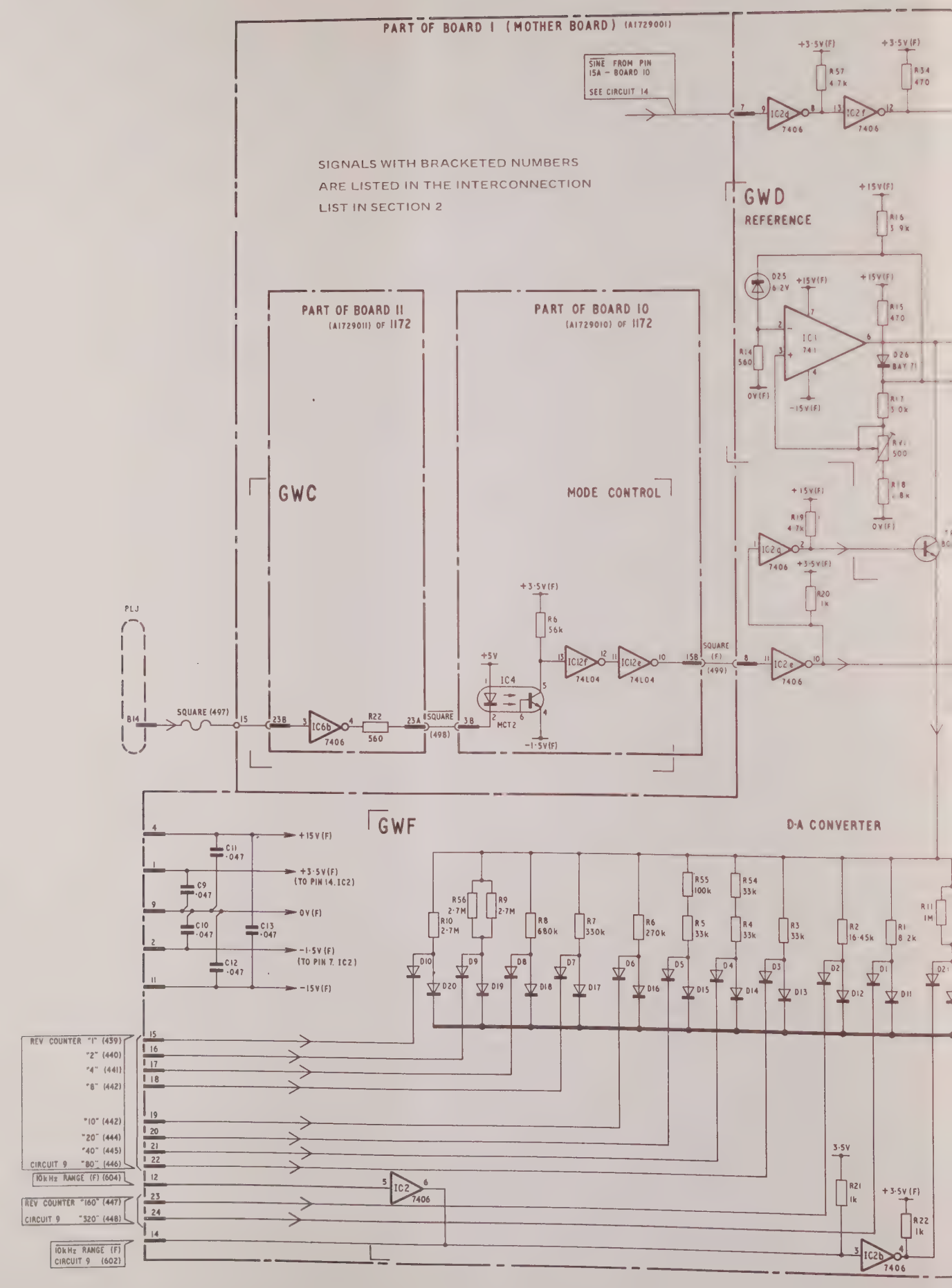


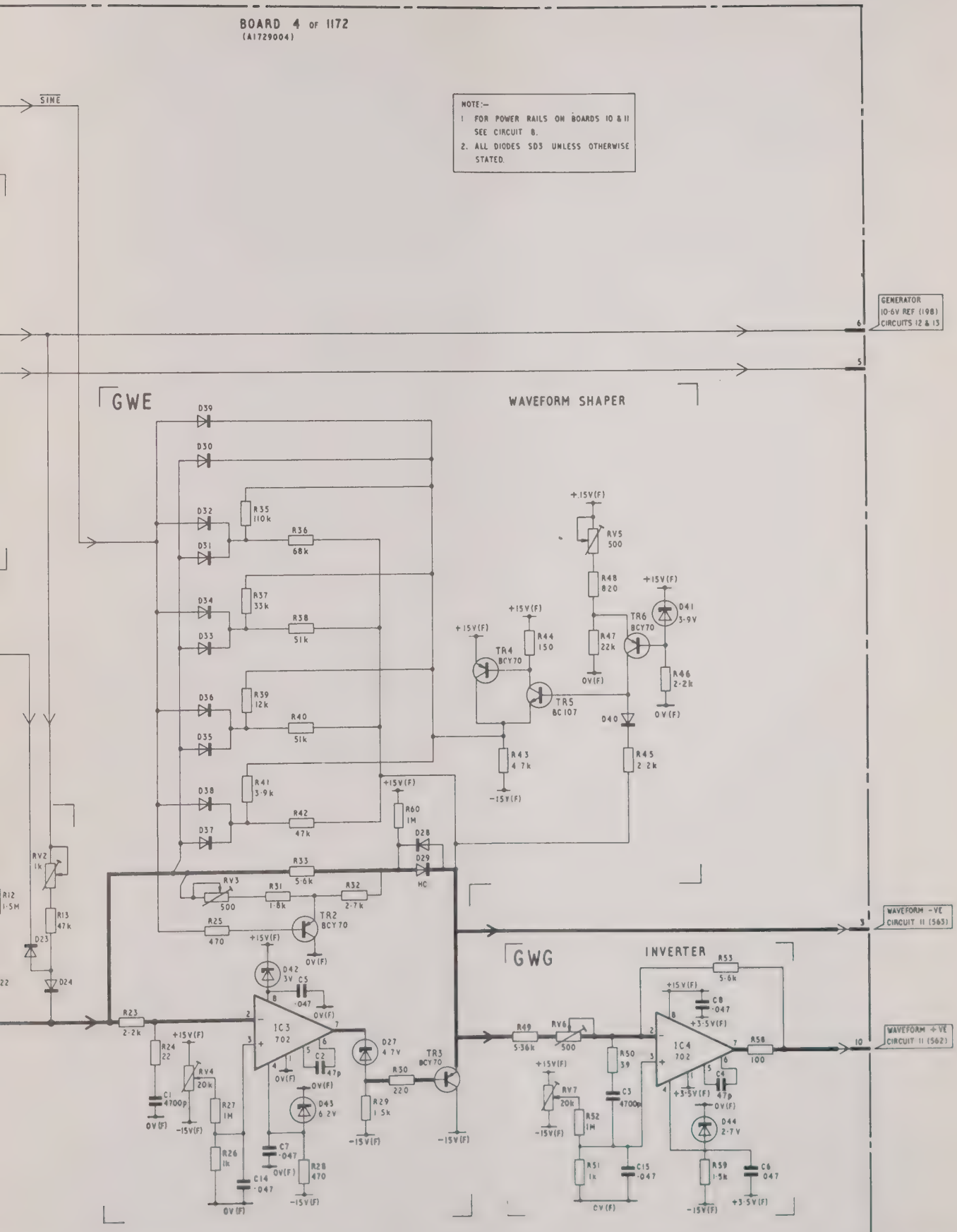
NOTE -
1 FOR POWER RAILS SEE CIRCUIT 9
2 ALL DIODES ARE SD3

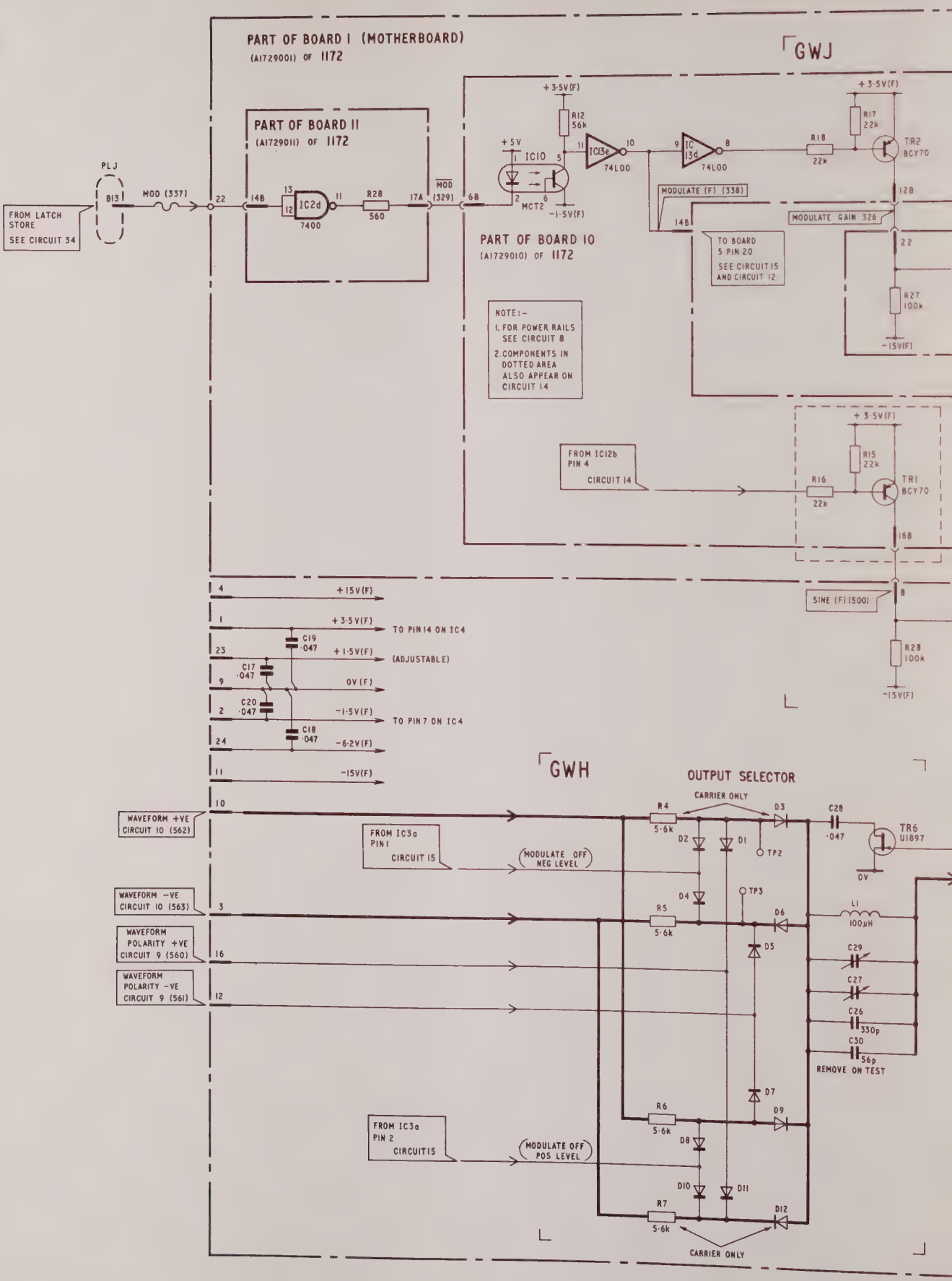


SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

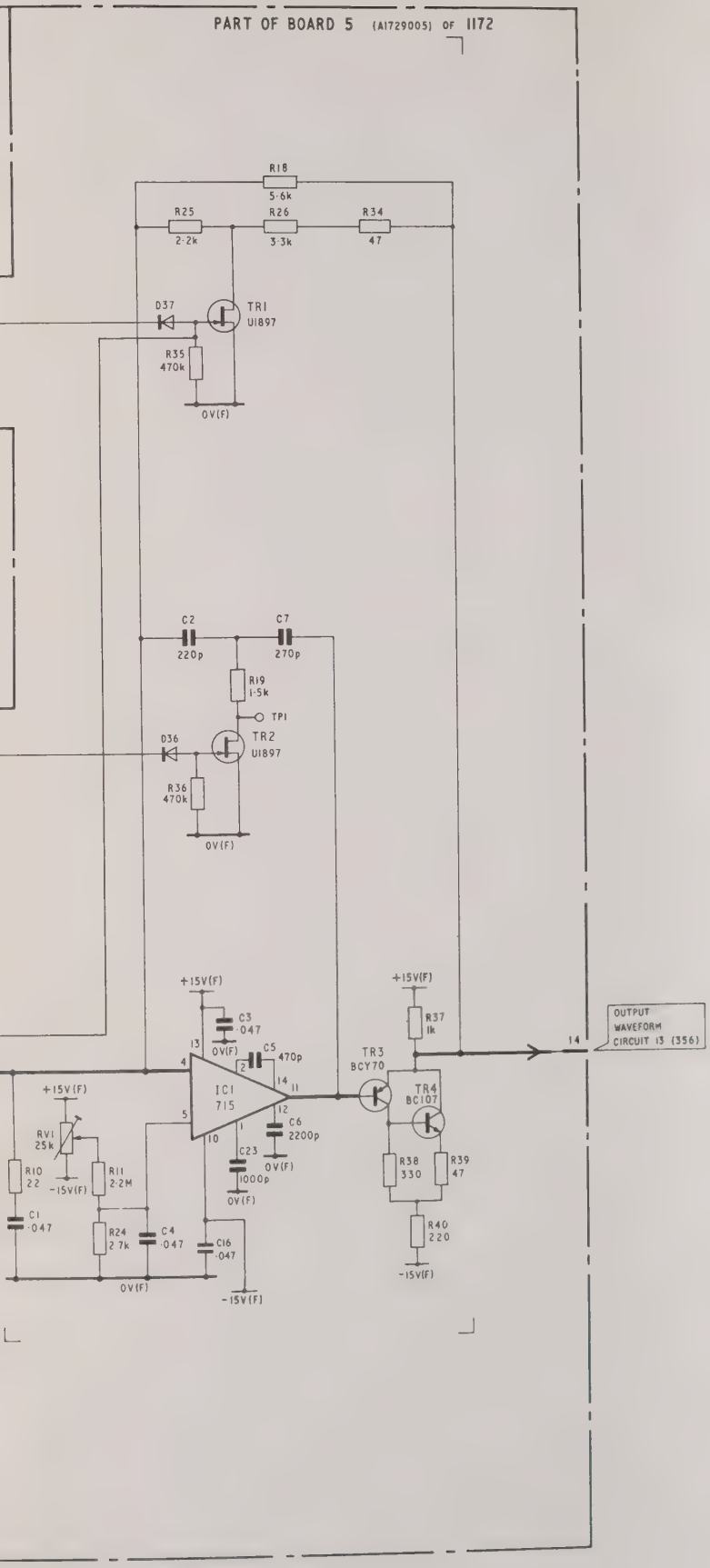

PART OF BOARD 3 (AI729003) OF 1172
REVERSIBLE COUNTER
UP
+3·5V(F)
R6 1k
7410
IC3c
7406
IC2d
IC11b
7476
R8 1k
(NOT USED)
REV COUNTER "1" (439)
"2" (440)
"4" (441)
CIRCUIT 10 "8" (442)
WAVEFORM POLARITY + ve (560) CIRCUIT 11
WAVEFORM POLARITY − ve (561) CIRCUIT 11
IC11a
7408
IC4a
IC12a
IC2b
R9 1k
R10 1k
PRE 0° (F) (390)
PRE 0° (F) (389)
R7 1k
IC2c
IC12b
REV COUNTER "10" (443)
"20" (444)
"40" (445)
CIRCUIT 10 "80" (446)
IC8c
REV COUNTER "160" (447)
CIRCUIT 10 "320" 448)
NOTE :-
FOR CLARITY R8 HAS BEEN DRAWN FOUR TIMES & IS SHOWN DOTTED IN THREE POSITIONS

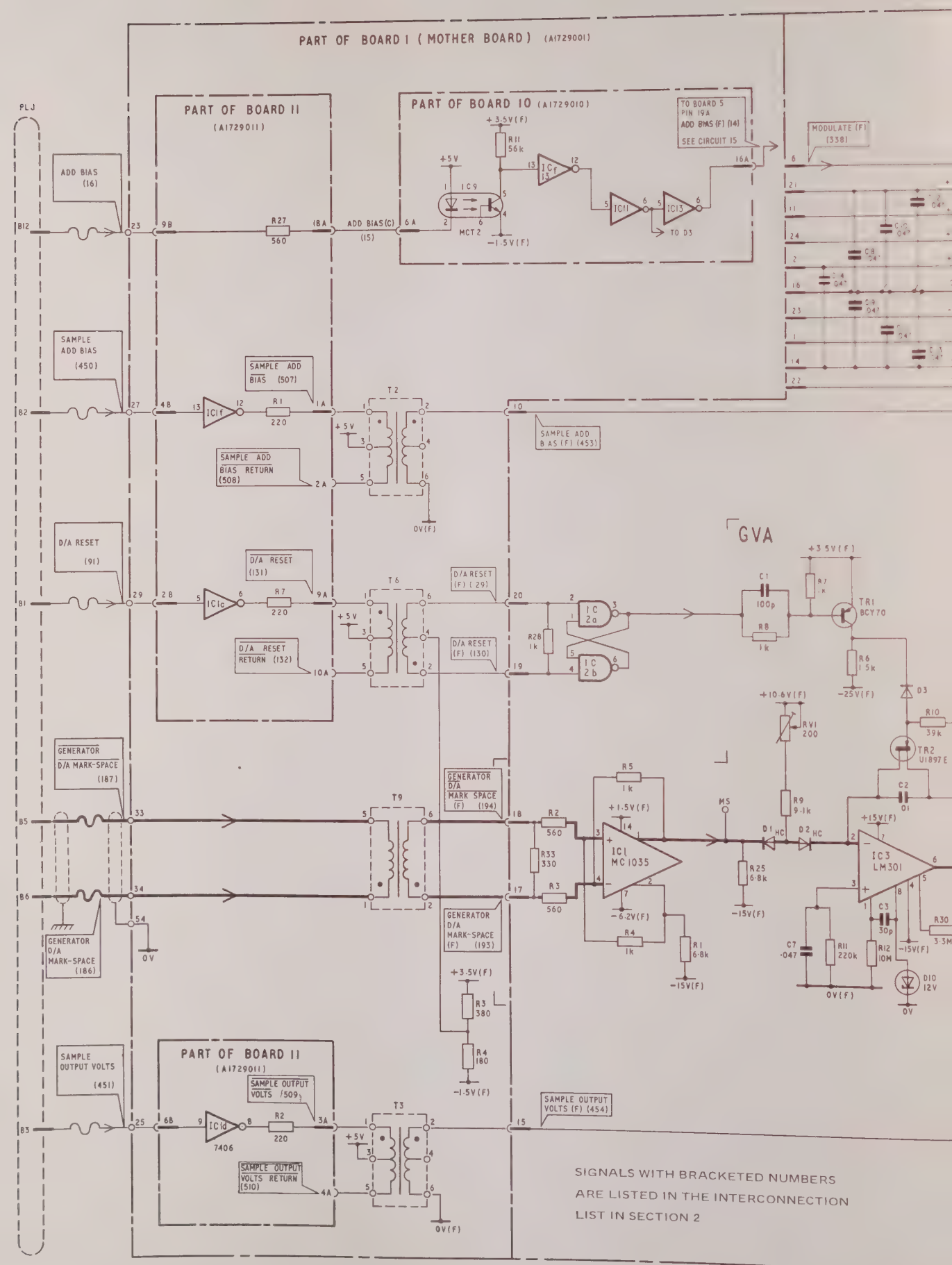

PART OF BOARD I (MOTHER BOARD) (A1729001)
SINE FROM PIN 15A – BOARD 10
SEE CIRCUIT 14
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2
GWD
REFERENCE
PART OF BOARD II (A1729011) OF 1172
PART OF BOARD 10 (A1729010) OF 1172
GWC
MODE CONTROL
PLJ
SQUARE (497)
SQUARE (498)
SQUARE (F) (499)
MCT2
GWF
D-A CONVERTER
+15V(F)
+3·5V(F)
0V(F)
-15V(F)
-1·5V(F)
+5V
(TO PIN 14. IC2)
(TO PIN 7. IC2)
REV COUNTER "1" (439)
"2" (440)
"4" (441)
"8" (442)
"10" (442)
"20" (444)
"40" (445)
CIRCUIT 9 "80" (446)
10kHz RANGE (F) (604)
REV COUNTER "160" (447)
CIRCUIT 9 "320" (448)
10kHz RANGE (F) CIRCUIT 9 (602)

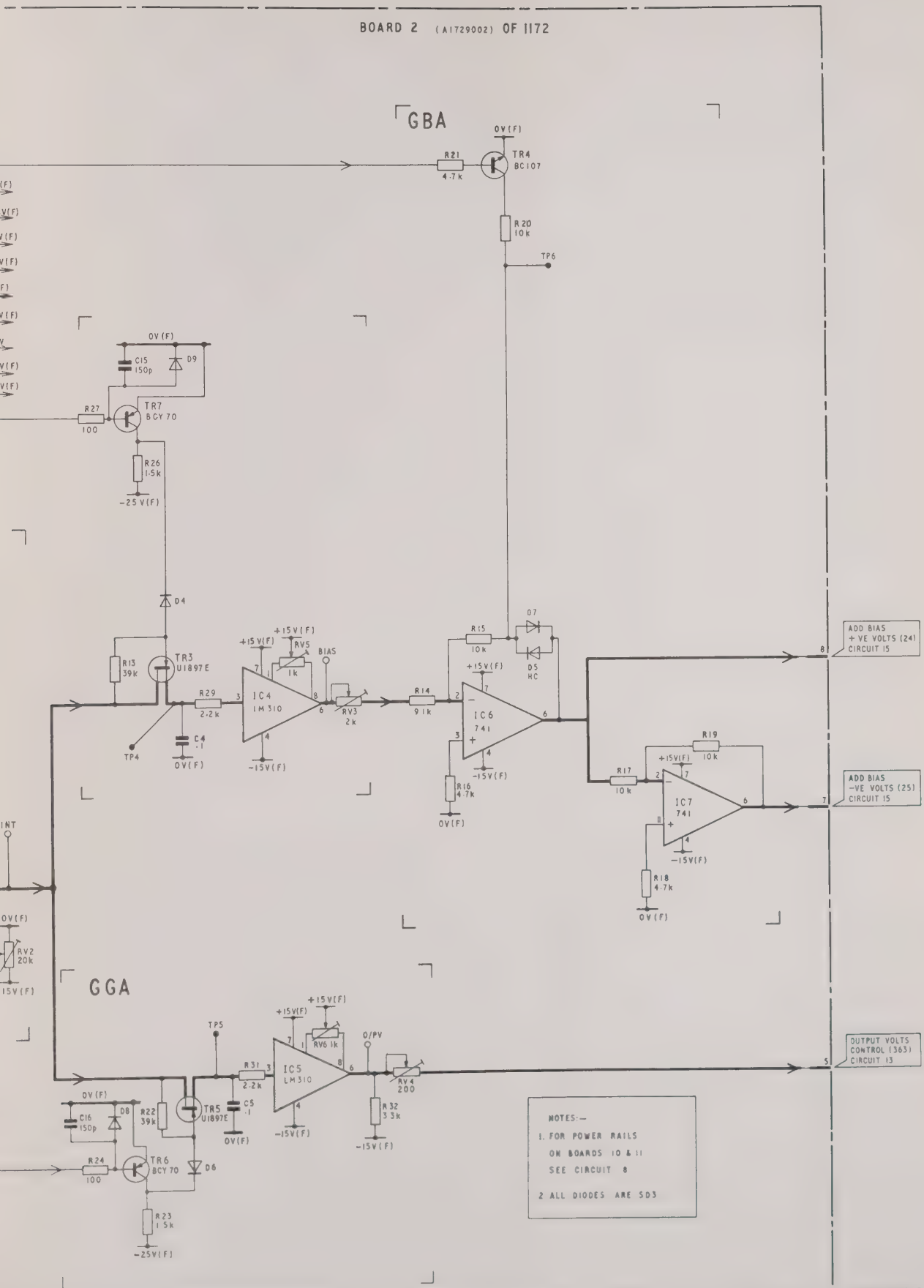

BOARD 4 OF 1172
(A1729004)
NOTE:-
1. FOR POWER RAILS ON BOARDS 10 & 11 SEE CIRCUIT 8.
2. ALL DIODES SD3 UNLESS OTHERWISE STATED.
SINE
GENERATOR 10·6V REF (198) CIRCUITS 12 & 13
GWE
WAVEFORM SHAPER
GWG
INVERTER
WAVEFORM -VE CIRCUIT 11 (563)
WAVEFORM +VE CIRCUIT 11 (562)
1C3 702
1C4 702
TR2 BCY70
TR3 BCY70
TR4 BCY70
TR5 BC107
TR6 BCY70
+15V(F)
-15V(F)
0V(F)
+3·5V(F)

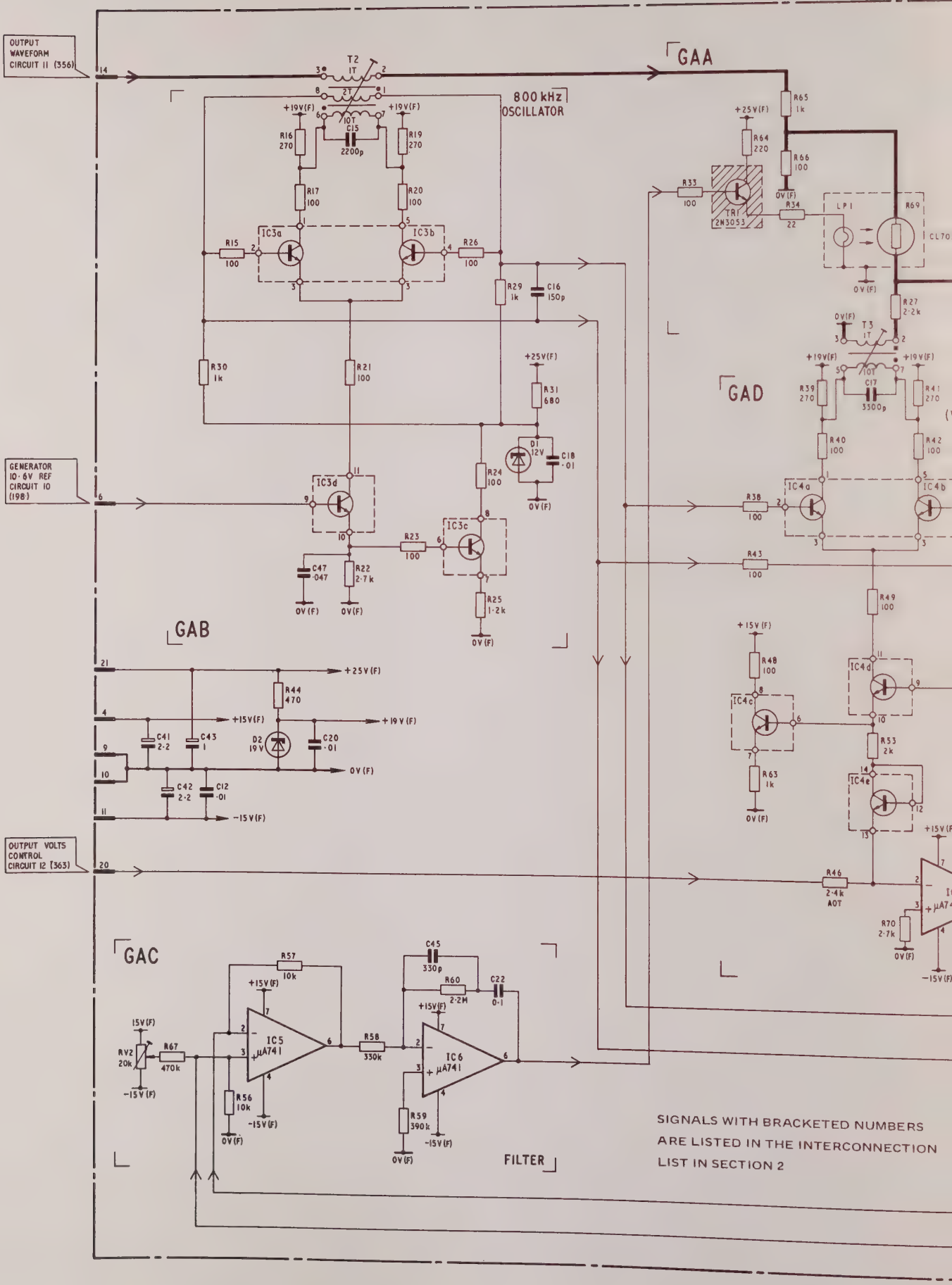


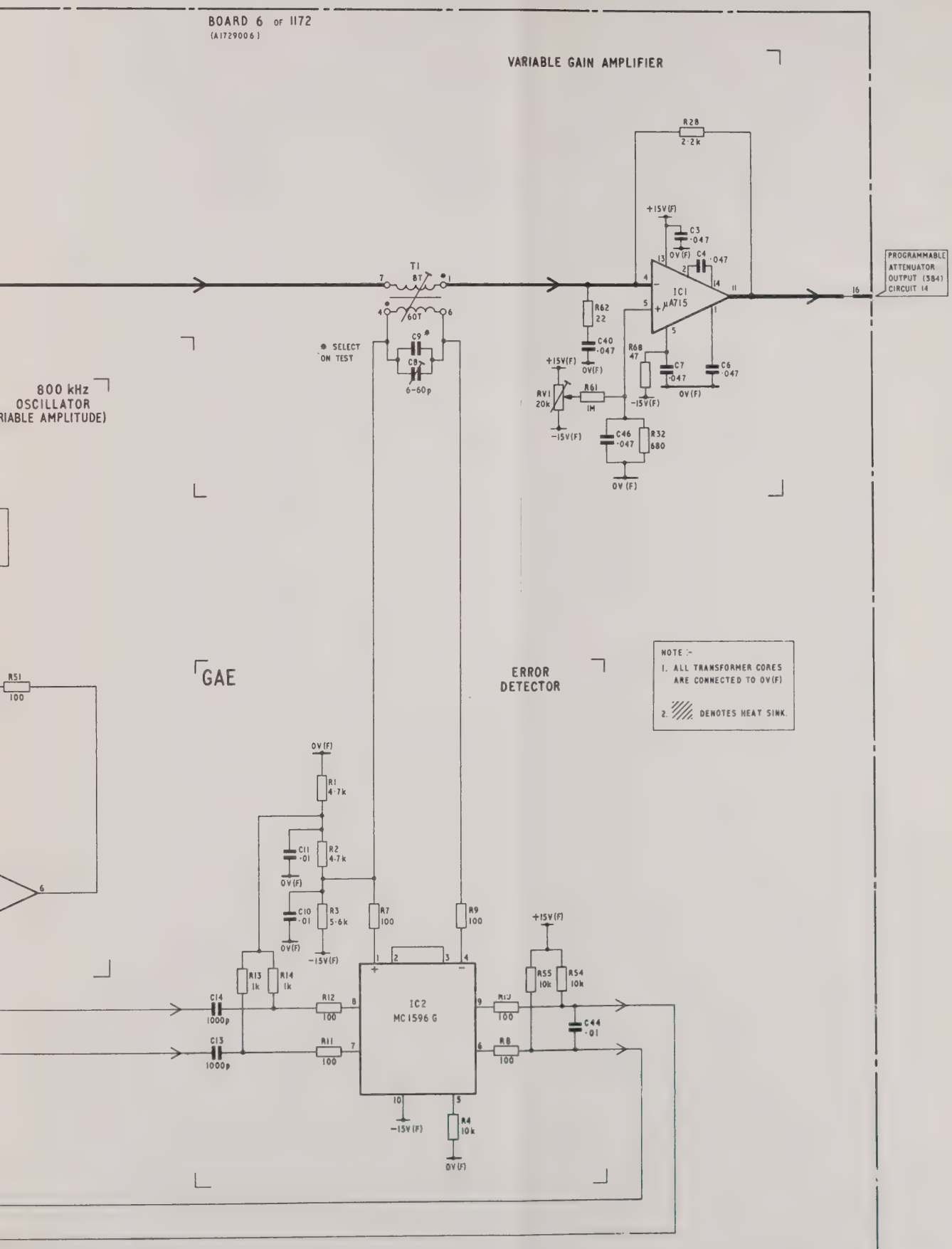
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

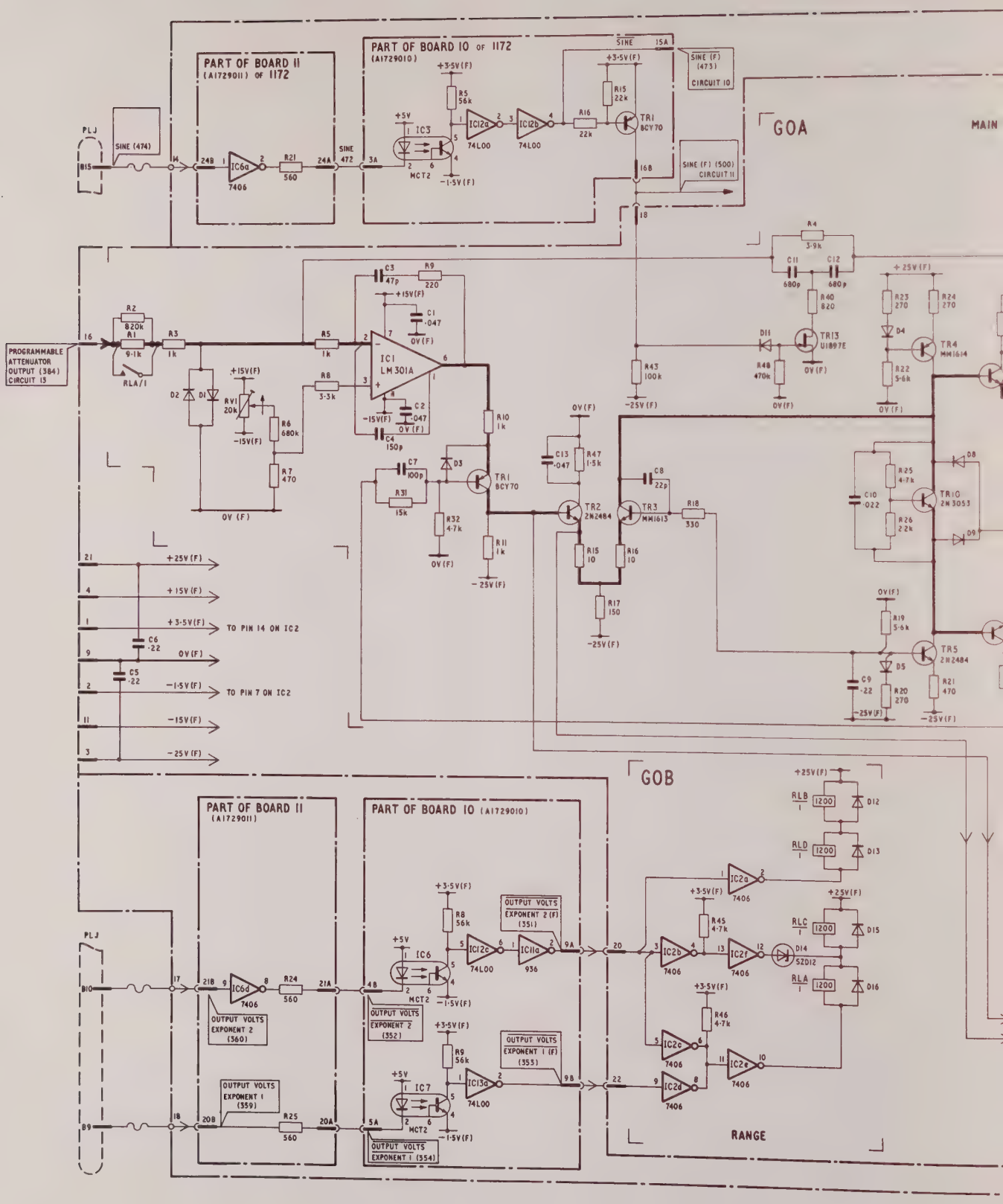

PART OF BOARD 5 (A1729005) OF 1172
R18
5·6k
R25
2·2k
R26
3·3k
R34
47
D37
TR1
U1897
R35
470k
0V(F)
C2
220p
C7
270p
R19
1·5k
TP1
D36
TR2
U1897
R36
470k
0V(F)
+15V(F)
C3
·047
0V(F)
C5
470p
IC1
715
+15V(F)
RV1
25k
-15V(F)
R10
22
R11
2·2M
C1
·047
R24
2·7k
C4
·047
C16
·047
0V(F)
-15V(F)
C6
2200p
C23
1000p
0V(F)
0V(F)
+15V(F)
R37
1k
TR3
BCY70
TR4
BC107
R38
330
R39
47
R40
220
-15V(F)
14
OUTPUT
WAVEFORM
CIRCUIT 13 (356)


PART OF BOARD I (MOTHER BOARD) (AI729001)
PART OF BOARD II (AI729011)
PART OF BOARD 10 (AI729010)
PLJ
ADD BIAS (16)
SAMPLE ADD BIAS (450)
D/A RESET (91)
GENERATOR D/A MARK-SPACE (187)
GENERATOR D/A MARK-SPACE (186)
SAMPLE OUTPUT VOLTS (451)
SAMPLE ADD BIAS (507)
SAMPLE ADD BIAS RETURN (508)
D/A RESET (131)
D/A RESET RETURN (132)
SAMPLE OUTPUT VOLTS /509\
SAMPLE OUTPUT VOLTS RETURN (510)
ADD BIAS (C) (15)
TO BOARD 5 PIN 19A ADD BIAS (F) (14)
SEE CIRCUIT 15
MODULATE (F) (338)
SAMPLE ADD BIAS (F) (453)
D/A RESET (F) (129)
D/A RESET (F) (130)
GENERATOR D/A MARK SPACE (F) (194)
GENERATOR D/A MARK-SPACE (F) (193)
SAMPLE OUTPUT VOLTS (F) (454)
TO D3
GVA
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

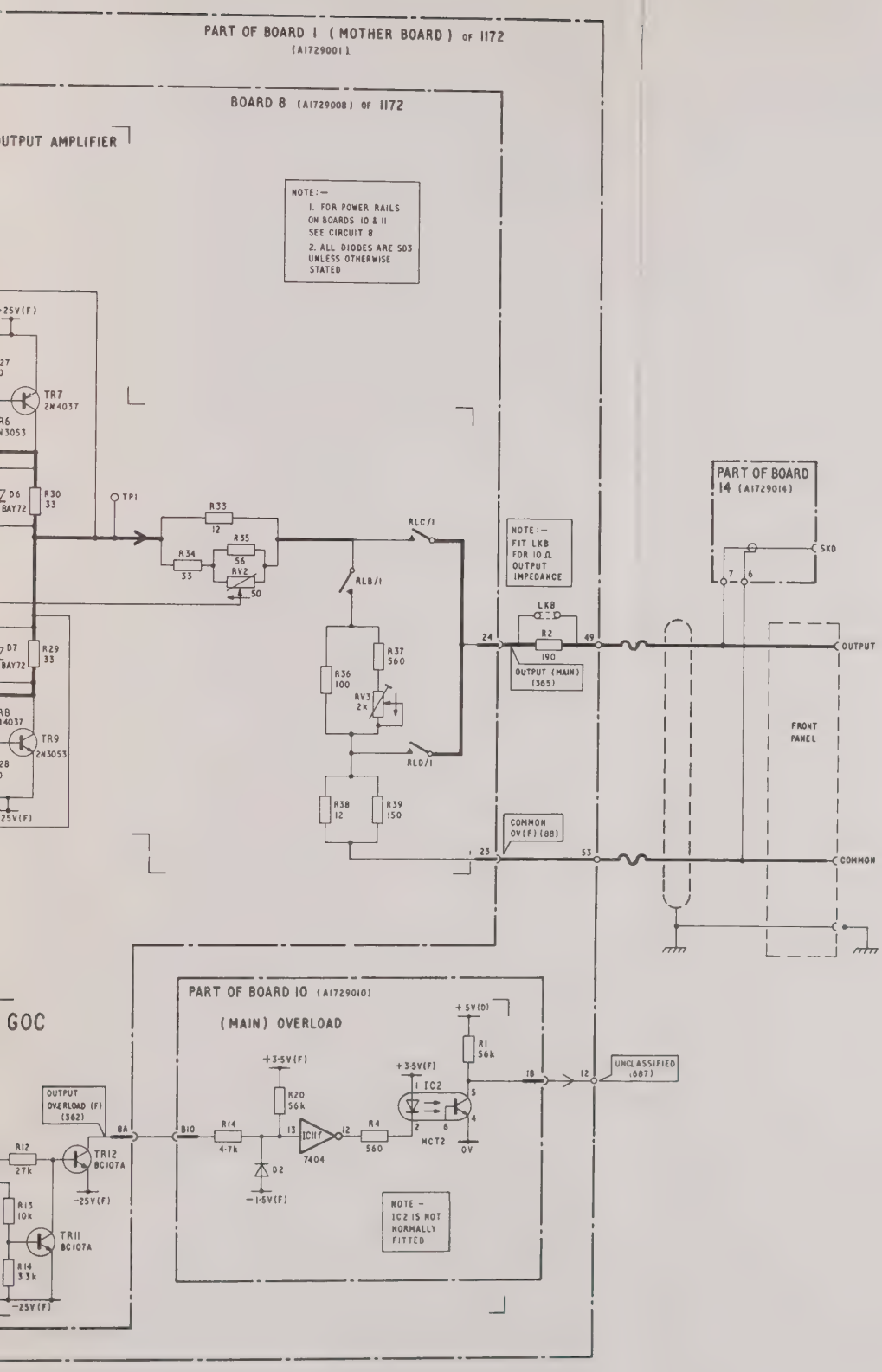

BOARD 2 (A1729002) OF 1172
GBA
0V(F)
R21
4.7k
TR4
BC107
R20
10k
TP6
0V(F)
C15
150p
D9
R27
100
TR7
BCY 70
R26
1.5k
-25V(F)
D4
R13
39k
TR3
U1897E
TP4
C4
.1
0V(F)
+15V(F)
+15V(F)
RV5
1k
BIAS
R29
2.2k
IC4
LM310
RV3
2k
-15V(F)
R14
9.1k
R15
10k
D7
D5
HC
+15V(F)
IC6
741
-15V(F)
R16
4.7k
0V(F)
ADD BIAS
+VE VOLTS (24)
CIRCUIT 15
R19
10k
+15V(F)
R17
10k
IC7
741
-15V(F)
R18
4.7k
0V(F)
ADD BIAS
-VE VOLTS (25)
CIRCUIT 15
INT
0V(F)
RV2
20k
15V(F)
GGA
+15V(F)
+15V(F)
TP5
RV6 1k
IC5
LM310
-15V(F)
O/PV
RV4
200
R32
3.3k
-15V(F)
R31
2.2k
C5
.1
0V(F)
TR5
U1897E
R22
39k
0V(F)
C16
150p
D8
R24
100
TR6
BCY 70
D6
R23
1.5k
-25V(F)
OUTPUT VOLTS
CONTROL (363)
CIRCUIT 13
NOTES:-
1. FOR POWER RAILS
ON BOARDS 10 & 11
SEE CIRCUIT 8
2 ALL DIODES ARE SD3


OUTPUT WAVEFORM CIRCUIT 11 (356)
GENERATOR 10·6V REF CIRCUIT 10 (198)
OUTPUT VOLTS CONTROL CIRCUIT 12 (363)
GAA
800 kHz OSCILLATOR
GAB
GAC
GAD
FILTER
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

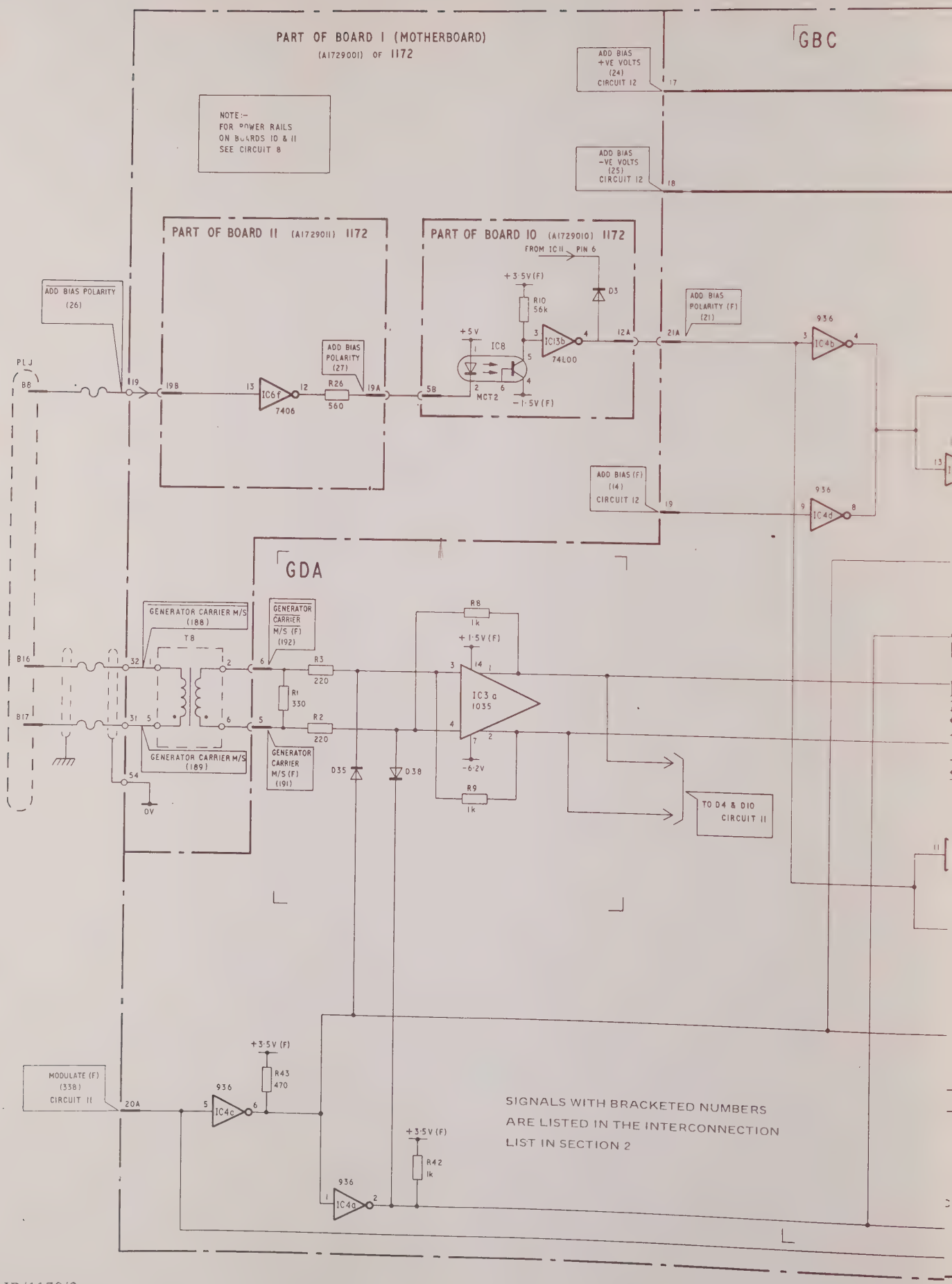

BOARD 6 OF 1172
(A1729006)
VARIABLE GAIN AMPLIFIER
R28
2·2k
+15V(F)
C3
·047
0V(F)
C4
·047
IC1
μA715
PROGRAMMABLE
ATTENUATOR
OUTPUT (384)
CIRCUIT 14
T1
8T
60T
* SELECT
ON TEST
C9 *
C8
6-60p
R62
22
C40
·047
0V(F)
R68
47
C7
·047
C6
·047
0V(F)
RV1
20k
R61
1M
-15V(F)
C46
·047
R32
680
0V(F)
800 kHz
OSCILLATOR
RIABLE AMPLITUDE)
GAE
ERROR
DETECTOR
NOTE :-
1. ALL TRANSFORMER CORES
ARE CONNECTED TO 0V(F)
2. DENOTES HEAT SINK.
R51
100
0V(F)
R1
4·7k
C11
·01
R2
4·7k
0V(F)
C10
·01
R3
5·6k
0V(F)
-15V(F)
R7
100
R9
100
+15V(F)
R13
1k
R14
1k
C14
1000p
C13
1000p
R12
100
R11
100
IC2
MC1596G
R55
10k
R54
10k
R10
100
R8
100
C44
·01
-15V(F)
R4
10k
0V(F)

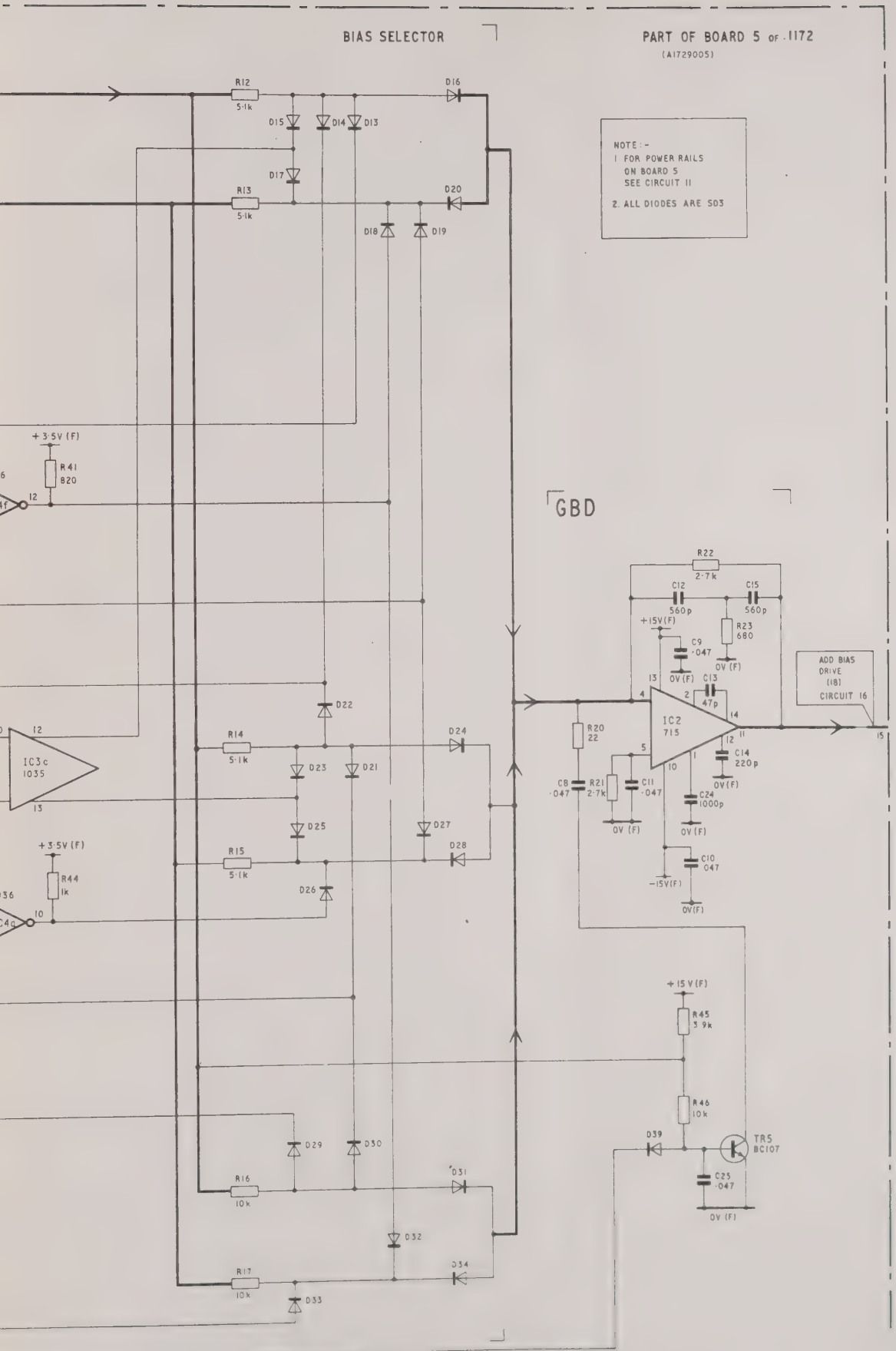


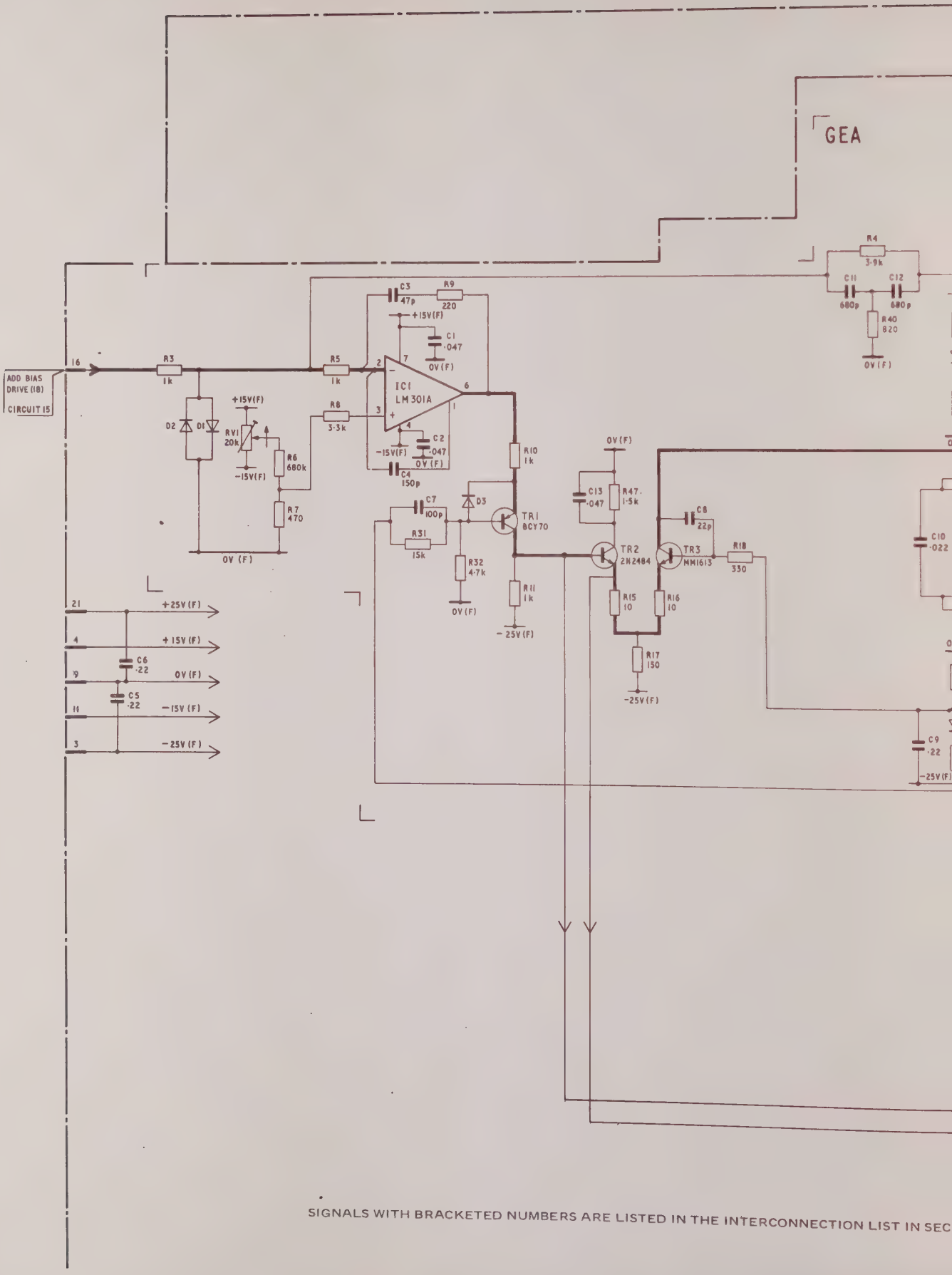
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST


PART OF BOARD 1 (MOTHER BOARD) OF 1172
(A1729001)
BOARD 8 (A1729008) OF 1172
UTPUT AMPLIFIER
NOTE:-
1. FOR POWER RAILS ON BOARDS 10 & 11 SEE CIRCUIT 8
2. ALL DIODES ARE S03 UNLESS OTHERWISE STATED
TR7 2N4037
R30 33
TP1
R33 12
R35 56
R34 33
RV2 50
RLC/1
RLB/1
RLD/1
R37 560
R36 100
RV3 2k
R38 12
R39 150
NOTE:- FIT LKB FOR 10Ω OUTPUT IMPEDANCE
LKB
R2 190
OUTPUT (MAIN) (365)
24
49
OUTPUT
PART OF BOARD 14 (A1729014)
SKO
7
6
FRONT PANEL
COMMON OV(F) (688)
23
53
COMMON
TR9 2N3053
R29 33
-25V(F)
PART OF BOARD 10 (A1729010)
(MAIN) OVERLOAD
+5V(D)
R1 56k
+3·5V(F)
R20 56k
IC1f
7404
R14 4·7k
R4 560
IC2
MCT2
OV
-1·5V(F)
D2
18
12
UNCLASSIFIED (687)
OUTPUT OVERLOAD (F) (362)
8A
8B
8C
TR12 BC107A
TR11 BC107A
R12 27k
R13 10k
R14 3·3k
-25V(F)
NOTE - IC2 IS NOT NORMALLY FITTED
GOC

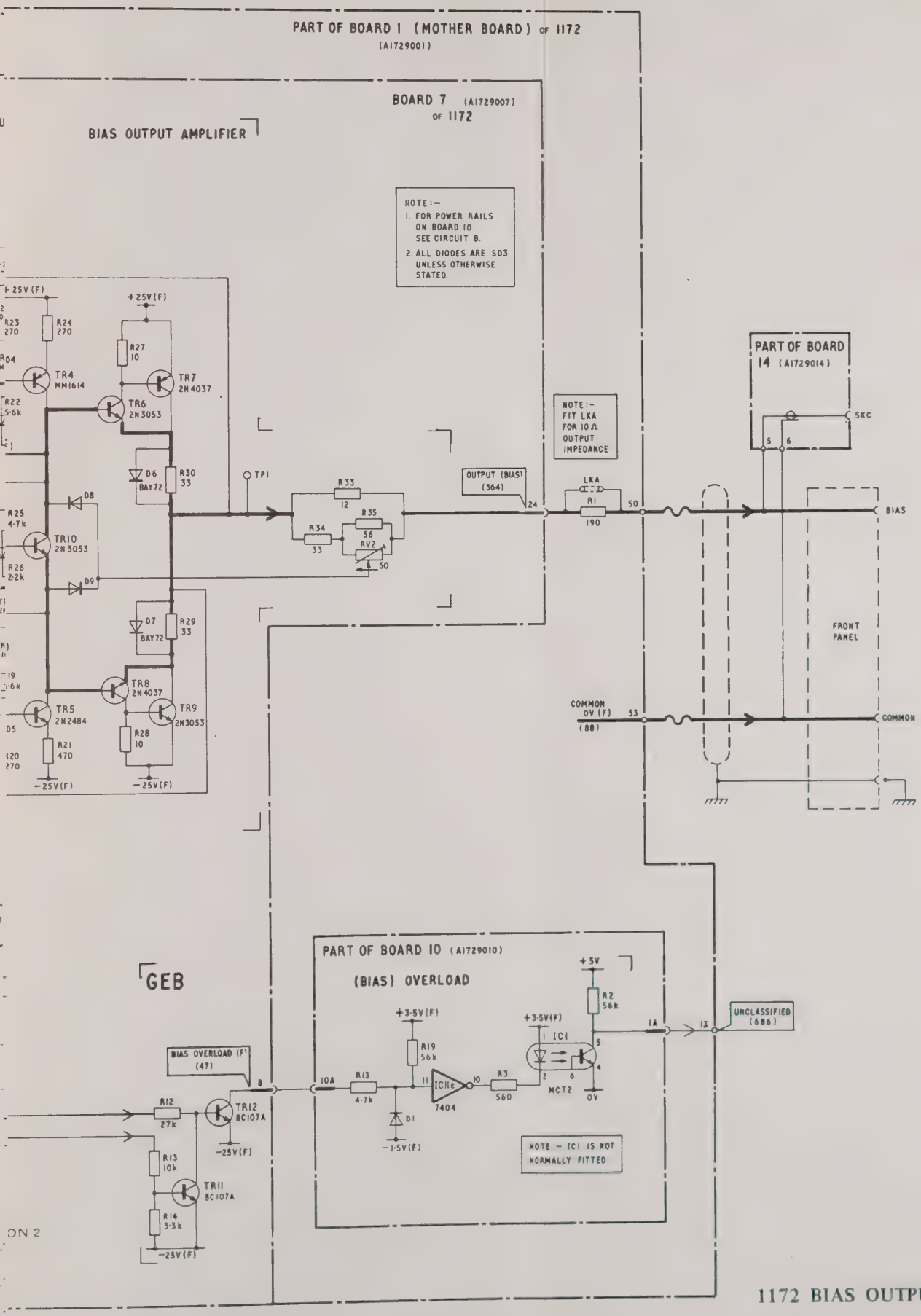
N SECTION 2


PART OF BOARD I (MOTHERBOARD)
(A1729001) OF 1172
GBC
NOTE:-
FOR POWER RAILS
ON BOARDS 10 & 11
SEE CIRCUIT 8
ADD BIAS
+VE VOLTS
(24)
CIRCUIT 12
17
ADD BIAS
-VE VOLTS
(25)
CIRCUIT 12
18
PART OF BOARD II (A1729011) 1172
PART OF BOARD 10 (A1729010) 1172
FROM IC11 PIN 6
+3·5V(F)
R10
56k
D3
ADD BIAS POLARITY
(26)
+5V
IC8
IC13b
74L00
MCT2
ADD BIAS POLARITY (F)
(21)
936
IC4b
PLJ
B8
19
19B
13
IC6f
7406
12
R26
560
19A
ADD BIAS POLARITY
(27)
5B
2
6
4
−1·5V(F)
12A
21A
ADD BIAS (F)
(14)
CIRCUIT 12
19
936
IC4d
GDA
GENERATOR CARRIER M/S
(188)
GENERATOR CARRIER
M/S (F)
(192)
T8
R8
1k
+1·5V(F)
B16
32
1
2
6
R3
220
R1
330
B17
31
5
6
5
R2
220
IC3a
1035
14
3
4
7
2
−6·2V
R9
1k
GENERATOR CARRIER M/S
(189)
GENERATOR
CARRIER
M/S (F)
(191)
54
0V
D35
D38
TO D4 & D10
CIRCUIT 11
MODULATE (F)
(338)
CIRCUIT 11
20A
+3·5V(F)
R43
470
936
IC4c
5
6
+3·5V(F)
R42
1k
936
IC4a
1
2
SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2

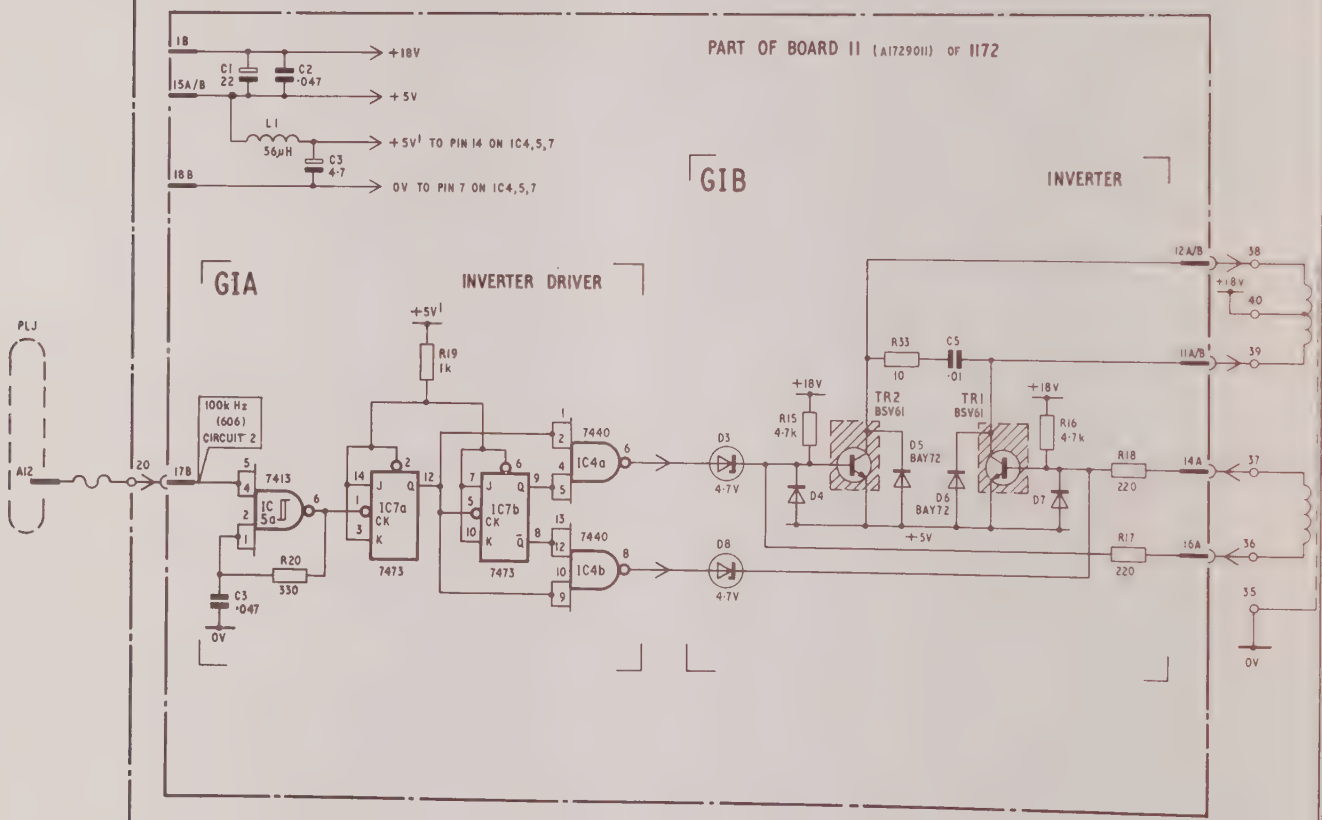

BIAS SELECTOR
PART OF BOARD 5 OF 1172
(A1729005)
NOTE :-
1 FOR POWER RAILS ON BOARD 5 SEE CIRCUIT 11
2. ALL DIODES ARE S03
GBD
R12 5·1k
R13 5·1k
R14 5·1k
R15 5·1k
R16 10k
R17 10k
D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31 D32 D33 D34
+3·5V (F)
R41 820
R44 1k
IC3c 1035
R22 2·7k
C12 560p
C15 560p
+15V(F)
R23 680
C9 ·047
0V (F)
C13 47p
IC2 715
R20 22
C8 ·047
R21 2·7k
C11 ·047
C14 220p
C24 1000p
C10 047
-15V(F)
ADD BIAS DRIVE (18) CIRCUIT 16
+15V(F)
R45 3·9k
R46 10k
D39
TR5 BC107
C25 ·047



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SEC

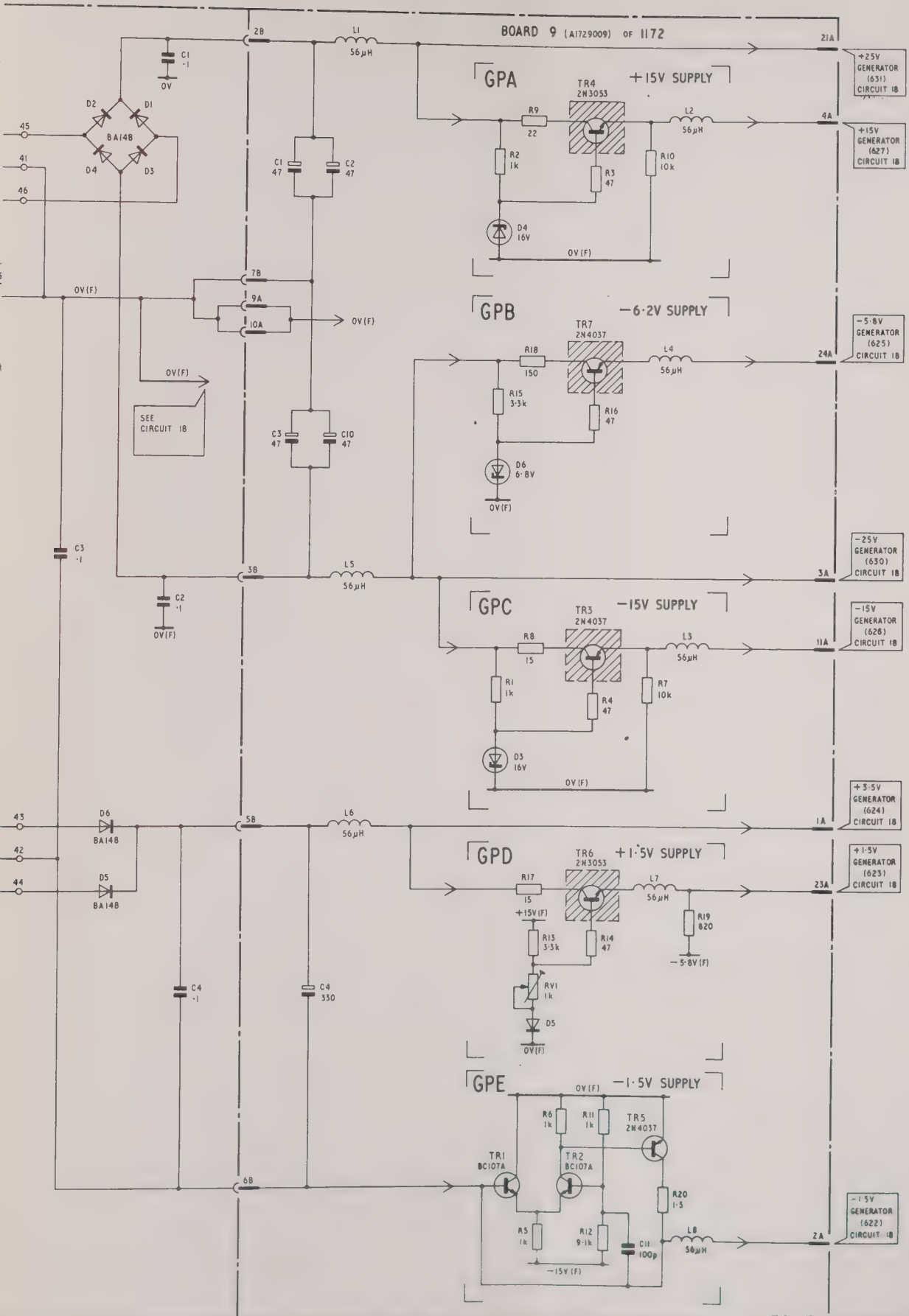

PART OF BOARD 1 (MOTHER BOARD) OF 1172
(A1729001)
BOARD 7 (A1729007)
OF 1172
BIAS OUTPUT AMPLIFIER
NOTE:-
1. FOR POWER RAILS ON BOARD 10 SEE CIRCUIT 8.
2. ALL DIODES ARE SD3 UNLESS OTHERWISE STATED.
+25V(F)
R23 270
R24 270
R27 10
TR4 MM1614
TR7 2N4037
TR6 2N3053
R22 5·6k
D6 BAY72
R30 33
TP1
R33 12
R35 56
RV2
R34 33
50
OUTPUT (BIAS) (364)
24
LKA
R1 190
50
NOTE:- FIT LKA FOR 10Ω OUTPUT IMPEDANCE
PART OF BOARD 14 (A1729014)
SKC
5
6
BIAS
FRONT PANEL
D8
R25 4·7k
TR10 2N3053
D9
R26 2·2k
D7 BAY72
R29 33
TR8 2N4037
TR5 2N2484
TR9 2N3053
R28 10
R21 470
-25V(F)
-25V(F)
COMMON 0V (F) (88)
53
COMMON
GEB
PART OF BOARD 10 (A1729010)
(BIAS) OVERLOAD
+5V
R2 56k
+3·5V(F)
R19 56k
+3·5V(F)
IC1
MCT2
5
4
2
6
0V
1A
13
UNCLASSIFIED (686)
BIAS OVERLOAD (F) (47)
8
10A
R13 4·7k
11
IC11c
7404
10
R3 560
D1
-1·5V(F)
R12 27k
TR12 BC107A
-25V(F)
R13 10k
TR11 BC107A
R14 3·3k
-25V(F)
NOTE:- IC1 IS NOT NORMALLY FITTED
ON 2

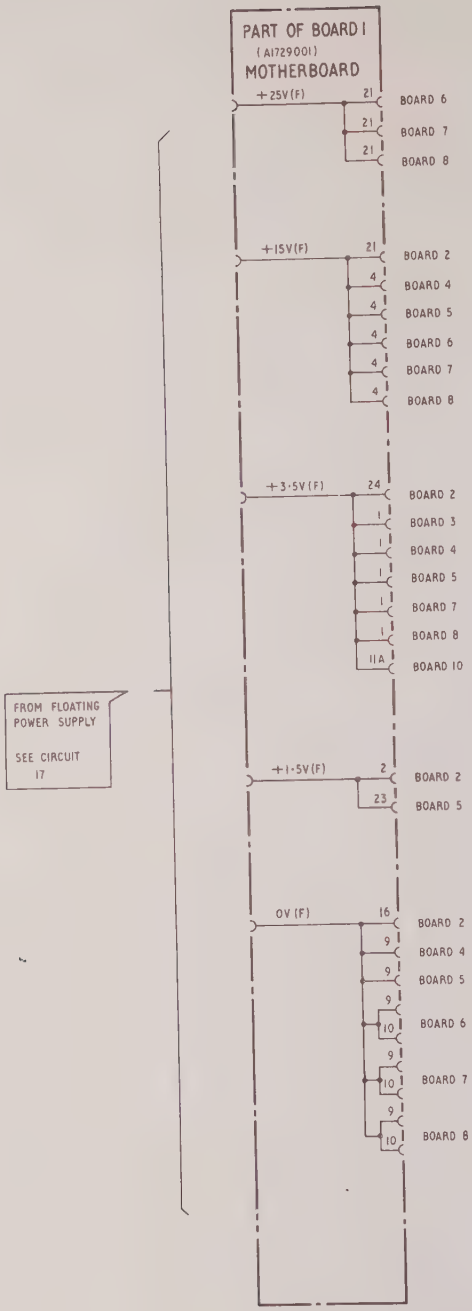
PART OF BOARD I (MOTHER BOARD) OF 1172
(A1729001)

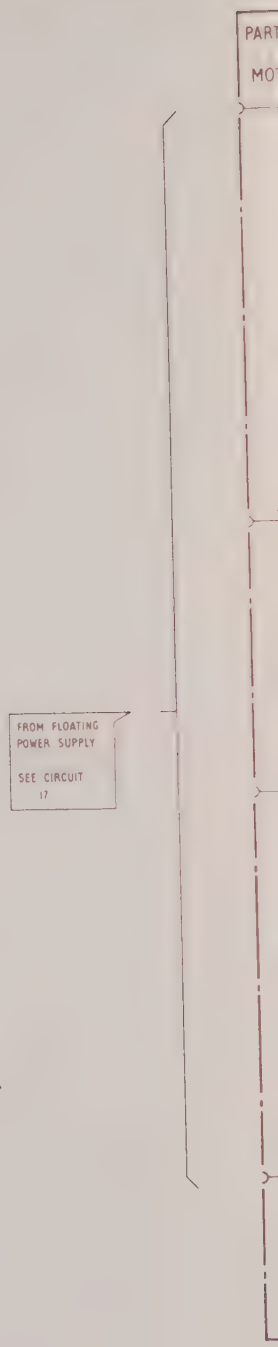


NOTE :-
1. SUFFIX (F) DENOTES A FLOATING SUPPLY E.G. +25V (F). WHERE NO SUFFIX IS GIVEN THE SUPPLY IS REFERENCED TO EARTH
2. DENOTES HEAT SINK
3. ALL DIODES SD3 UNLESS OTHERWISE STATED

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

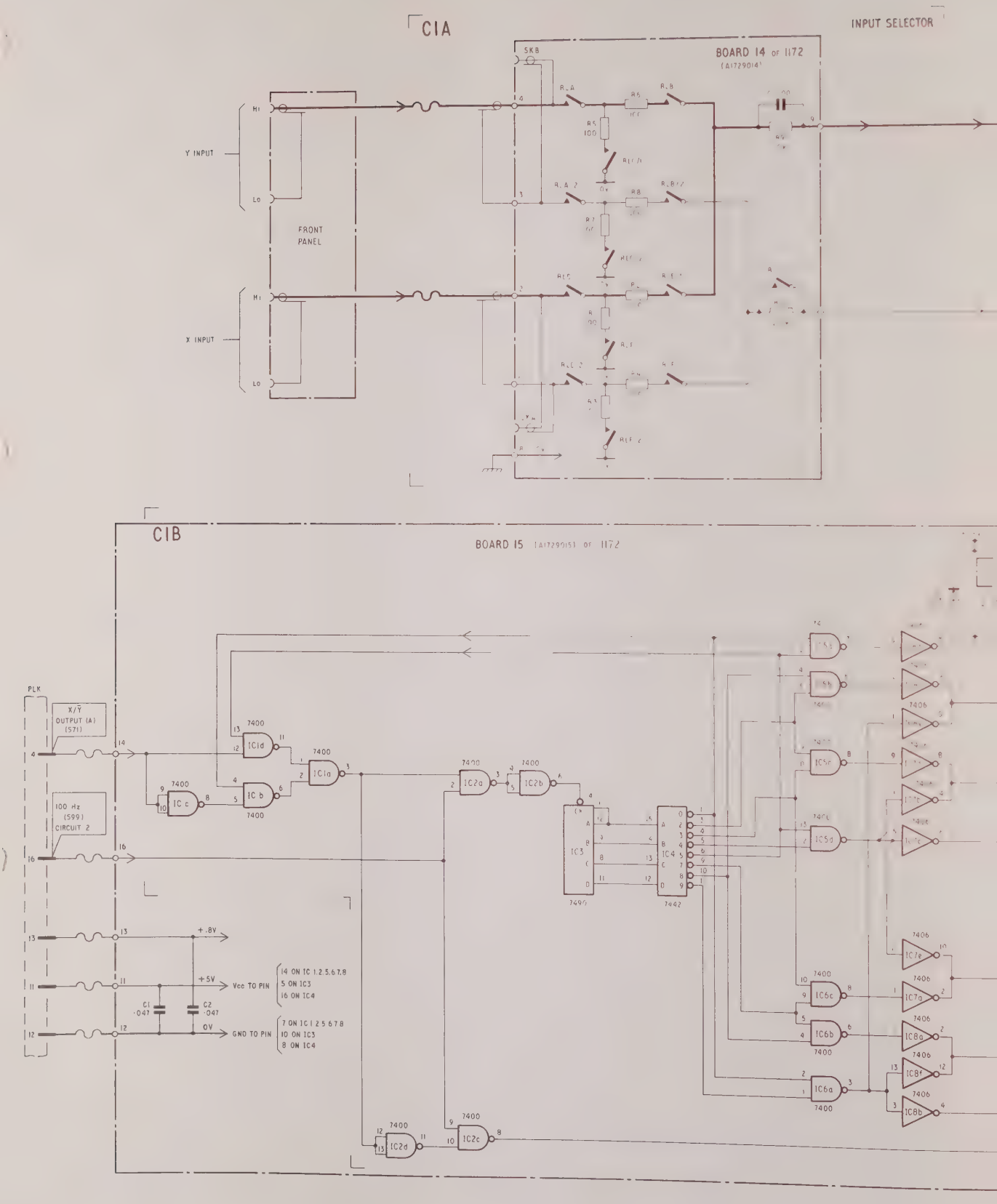

BOARD 9 (A1729009) OF 1172
GPA +15V SUPPLY
GPB −6·2V SUPPLY
GPC −15V SUPPLY
GPD +1·5V SUPPLY
GPE −1·5V SUPPLY
TR4 2N3053
TR7 2N4037
TR3 2N4037
TR6 2N3053
TR5 2N4037
TR1 BC107A
TR2 BC107A
D1 D2 D3 D4
BA148
D4 16V
D6 6·8V
D3 16V
D5
RV1 1k
L1 56µH
L2 56µH
L3 56µH
L4 56µH
L5 56µH
L6 56µH
L7 56µH
L8 56µH
R9 22
R2 1k
R3 47
R10 10k
R18 150
R15 3·3k
R16 47
R8 15
R1 1k
R4 47
R7 10k
R17 15
R13 3·3k
R14 47
R19 820
R6 1k
R11 1k
R20 1·5
R5 1k
R12 9·1k
C11 100p
C1 ·1
C1 47
C2 47
C3 47
C10 47
C3 ·1
C2 ·1
C4 ·1
C4 330
+25V GENERATOR (631) CIRCUIT 18
+15V GENERATOR (627) CIRCUIT 18
−5·8V GENERATOR (625) CIRCUIT 18
−25V GENERATOR (630) CIRCUIT 18
−15V GENERATOR (628) CIRCUIT 18
+3·5V GENERATOR (624) CIRCUIT 18
+1·5V GENERATOR (623) CIRCUIT 18
−1·5V GENERATOR (622) CIRCUIT 18
SEE CIRCUIT 18
0V
0V(F)
+15V(F)
−15V(F)
−5·8V(F)
2B 3B 5B 6B 7B 9A 10A
21A 4A 24A 3A 11A 1A 23A 2A
45 41 46 43 42 44



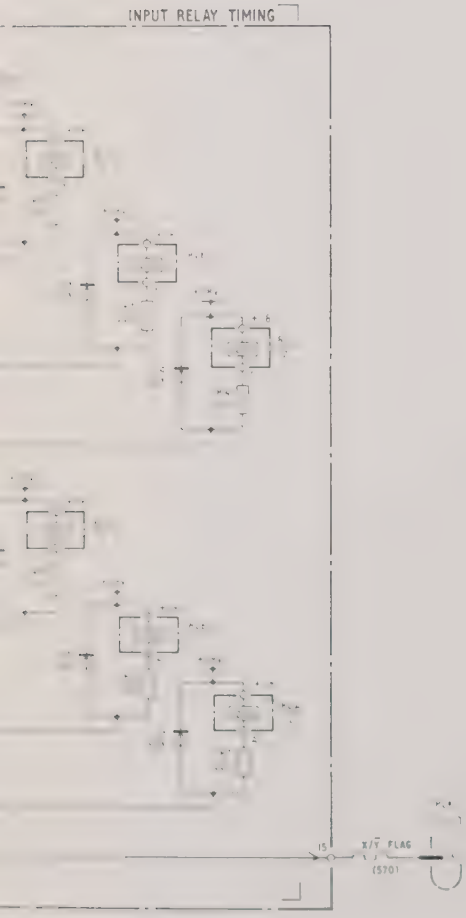


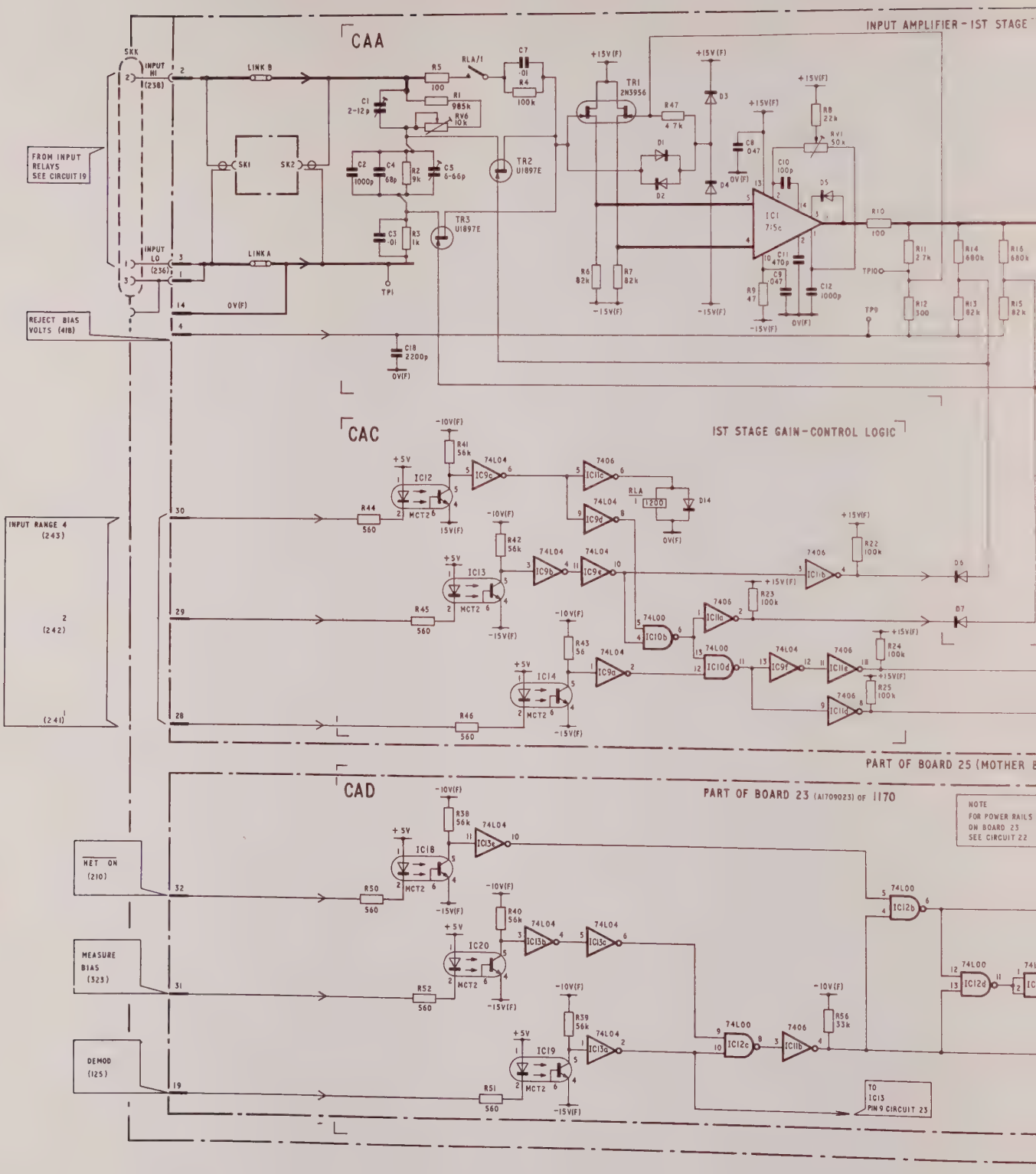
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

OF BOARD I
729001)
HERBOARD
V(F)
23
BOARD 2
2
BOARD 3
2
BOARD 4
2
BOARD 5
2
BOARD 7
2
BOARD 8
11B
BOARD 10
2V(F)
1
BOARD 2
24
BOARD 5
V(F)
14
BOARD 2
11
BOARD 4
11
BOARD 5
11
BOARD 6
11
BOARD 7
11
BOARD 8
V(F)
22
BOARD 2
3
BOARD 6
3
BOARD 7
3
BOARD 8

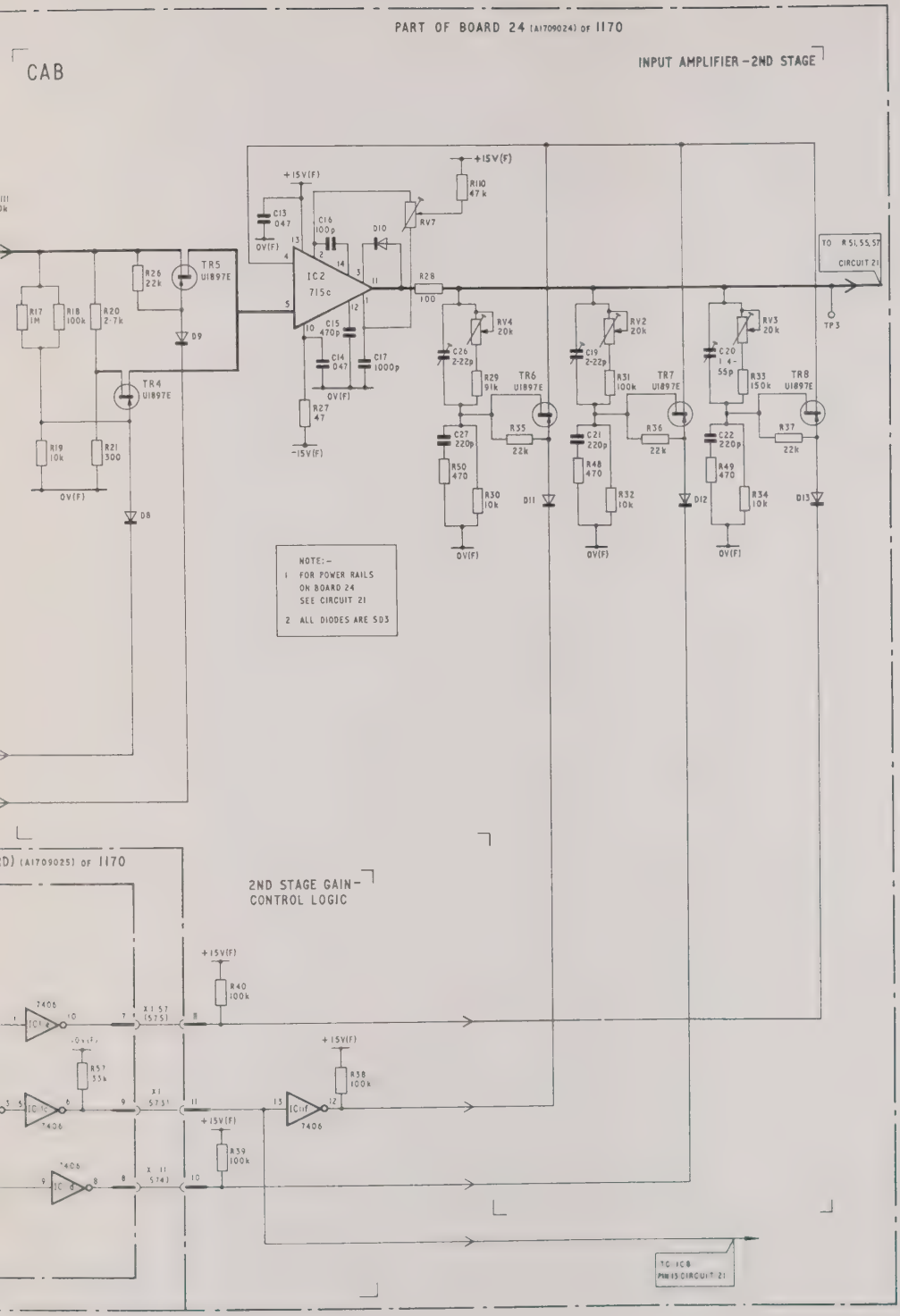


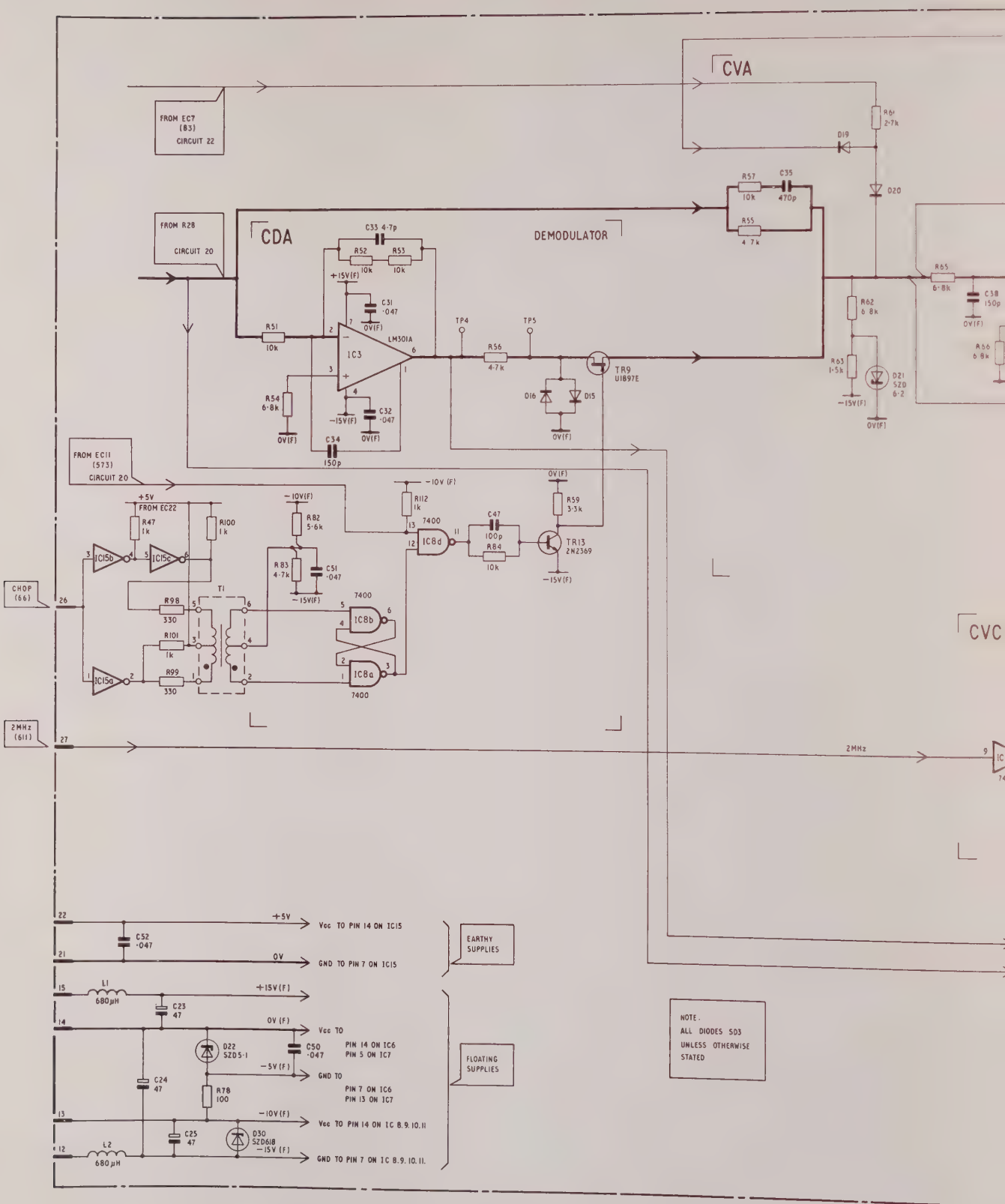
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


INPUT RELAY TIMING
X/Y FLAG
(5701)

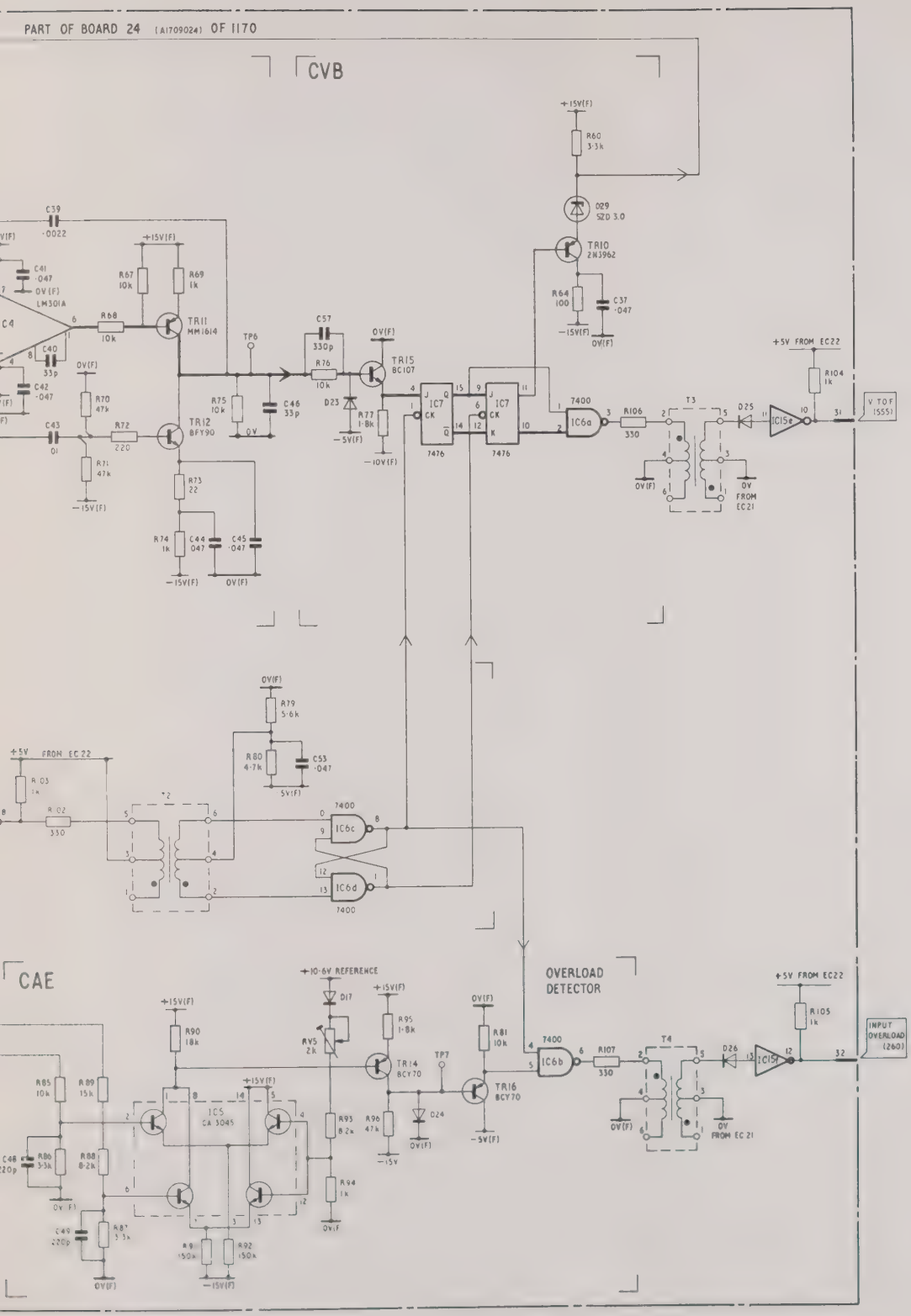


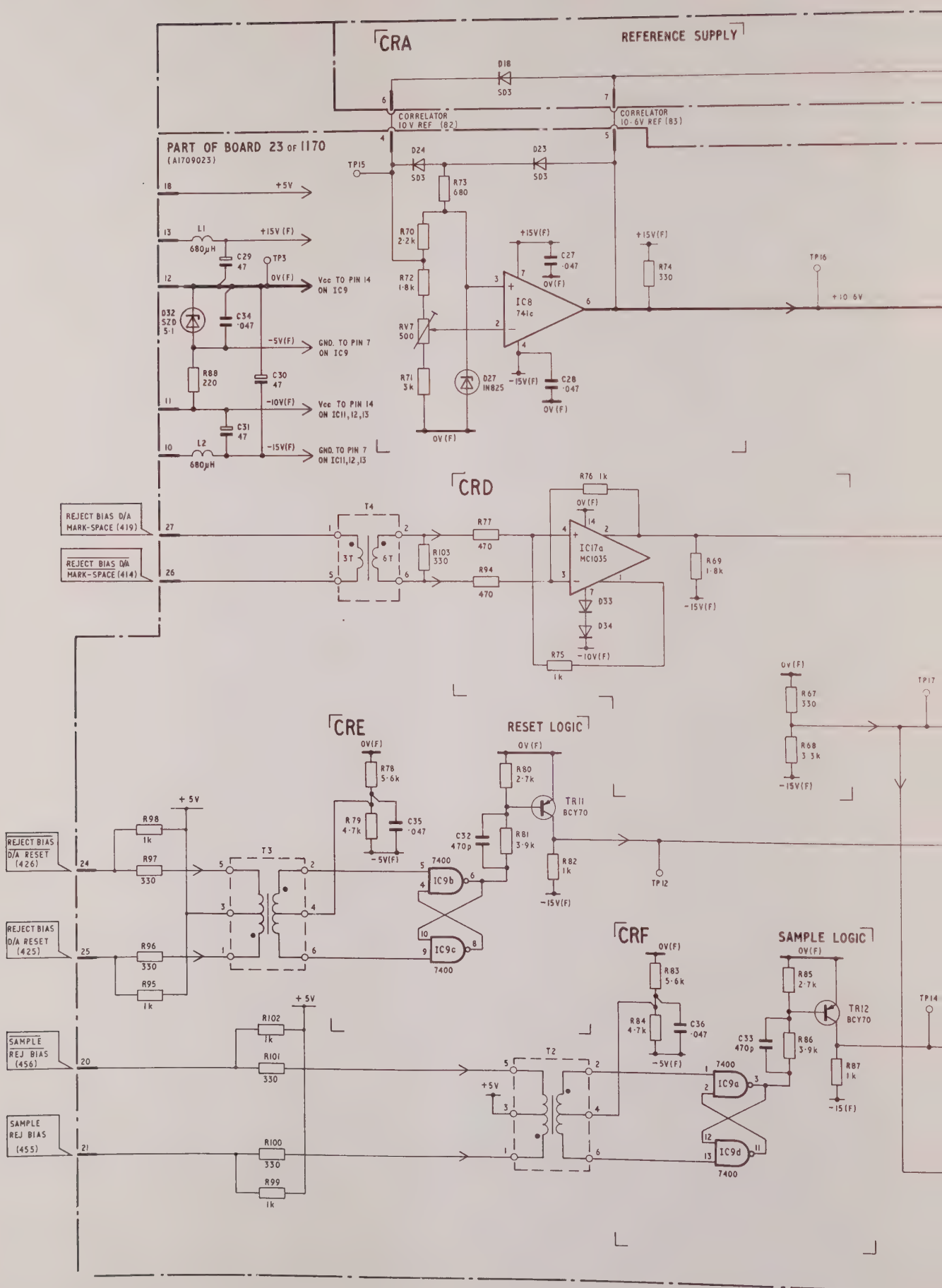
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTIO


PART OF BOARD 24 (A1709024) OF 1170
CAB
INPUT AMPLIFIER – 2ND STAGE
+15V(F)
R110 47k
C13 047
C16 100p
D10
RV7
IC2 715c
R28 100
TO R51,55,57 CIRCUIT 21
TP3
TR5 U1897E
R26 22k
R17 1M
R18 100k
R20 2·7k
D9
TR4 U1897E
R19 10k
R21 300
D8
C15 470p
C14 047
C17 1000p
R27 47
-15V(F)
0V(F)
RV4 20k
C26 2-22p
R29 91k
TR6 U1897E
R35 22k
C27 220p
R50 470
R30 10k
D11
RV2 20k
C19 2-22p
R31 100k
TR7 U1897E
R36 22k
C21 220p
R48 470
R32 10k
D12
RV3 20k
C20 1·4-55p
R33 150k
TR8 U1897E
R37 22k
C22 220p
R49 470
R34 10k
D13
NOTE:-
1 FOR POWER RAILS ON BOARD 24 SEE CIRCUIT 21
2 ALL DIODES ARE 503
2ND STAGE GAIN-CONTROL LOGIC
(A1709025) OF 1170
R40 100k
7406
R57 33k
R38 100k
R39 100k
TO IC8 PINS CIRCUIT 21



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


PART OF BOARD 24 (A1709024) OF 1170
CVB
CAE
OVERLOAD DETECTOR
+15V(F)
R60 3·3k
D29 SZD 3.0
TR10 2N3962
R64 100
C37 ·047
C39 ·0022
C41 ·047
LM301A
R67 10k
R69 1k
R68 10k
TR11 MM1614
C40 33p
C42 ·047
C43 ·01
R70 47k
R71 47k
TR12 BFY90
R72 220
R73 22
R74 1k
C44 ·047
C45 ·047
TP6
C57 330p
R76 10k
D23
R77 1·8k
TR15 BC107
R75 10k
C46 33p
IC7 7476
IC7 7476
7400 IC6a
R106 330
T3
D25
IC15e
+5V FROM EC22
R104 1k
V TO F (555)
0V FROM EC21
R79 5·6k
R80 4·7k
C53 ·047
+5V FROM EC22
R03
R02 330
T2
7400 IC6c
IC6d
+10·6V REFERENCE
D17
RV5 2k
R95 1·8k
TR14 BCY70
TP7
R81 10k
TR16 BCY70
IC6b
R107 330
T4
D26
IC15f
+5V FROM EC22
R105 1k
INPUT OVERLOAD (260)
R90 18k
R85 10k
R89 15k
R86 3·3k
R88 8·2k
R87 5·3k
C49 ·22p
IC5 CA 3045
R93 8·2k
R96 47k
D24
R94 1k
R91 150k
R92 150k
-15V
-5V(F)
-10V(F)
0V(F)

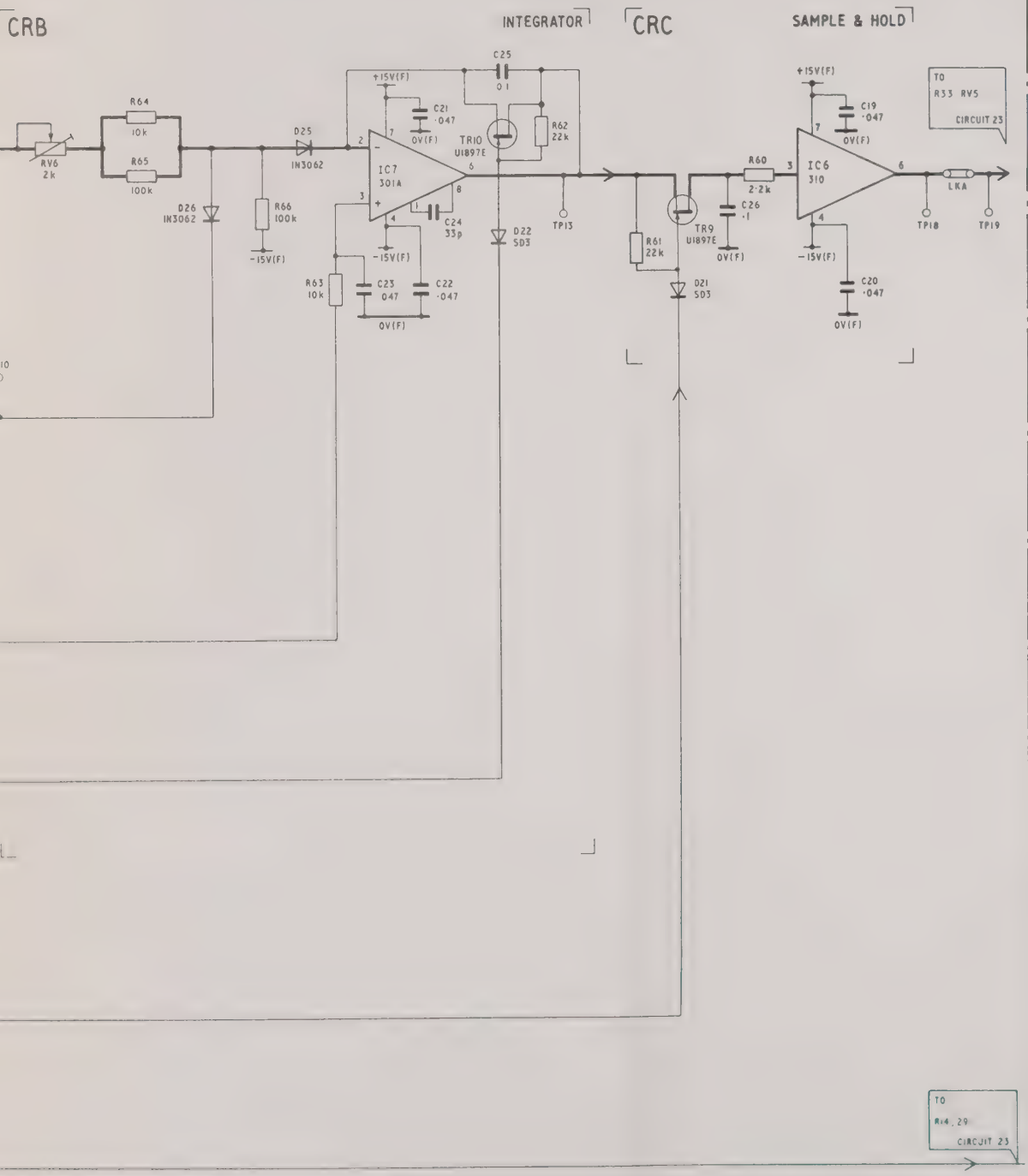

CRA
REFERENCE SUPPLY
PART OF BOARD 23 OF 1170
(A1709023)
D18
SD3
CORRELATOR 10 V REF (82)
CORRELATOR 10·6V REF (83)
D24
D23
TP15
R73 680
+5V
L1 680µH
+15V(F)
C29 47
TP3
0V(F)
Vcc TO PIN 14 ON IC9
D32 SZD 5·1
C34 ·047
-5V(F)
GND. TO PIN 7 ON IC9
R88 220
C30 47
-10V(F)
Vcc TO PIN 14 ON IC11,12,13
C31 47
-15V(F)
GND. TO PIN 7 ON IC11,12,13
L2 680µH
R70 2·2k
R72 1·8k
RV7 500
R71 3k
D27 IN825
IC8 741c
C27 ·047
C28 ·047
R74 330
TP16
+10·6V
CRD
REJECT BIAS D/A MARK-SPACE (419)
REJECT BIAS D/A MARK-SPACE (414)
T4
3T
6T
R77 470
R94 470
R103 330
R76 1k
IC17a MC1035
R69 1·8k
D33
D34
R75 1k
CRE
RESET LOGIC
R78 5·6k
R79 4·7k
C35 ·047
R80 2·7k
TR11 BCY70
C32 470p
R81 3·9k
R82 1k
TP12
R67 330
R68 3·3k
TP17
+5V
R98 1k
R97 330
R96 330
R95 1k
T3
REJECT BIAS D/A RESET (426)
REJECT BIAS D/A RESET (425)
7400
IC9b
IC9c
CRF
SAMPLE LOGIC
R83 5·6k
R84 4·7k
C36 ·047
R85 2·7k
TR12 BCY70
C33 470p
R86 3·9k
R87 1k
TP14
R102 1k
R101 330
R100 330
R99 1k
T2
SAMPLE REJ BIAS (456)
SAMPLE REJ BIAS (455)
IC9a
IC9d

PART OF BOARD 24 (AI709024) OF 1170

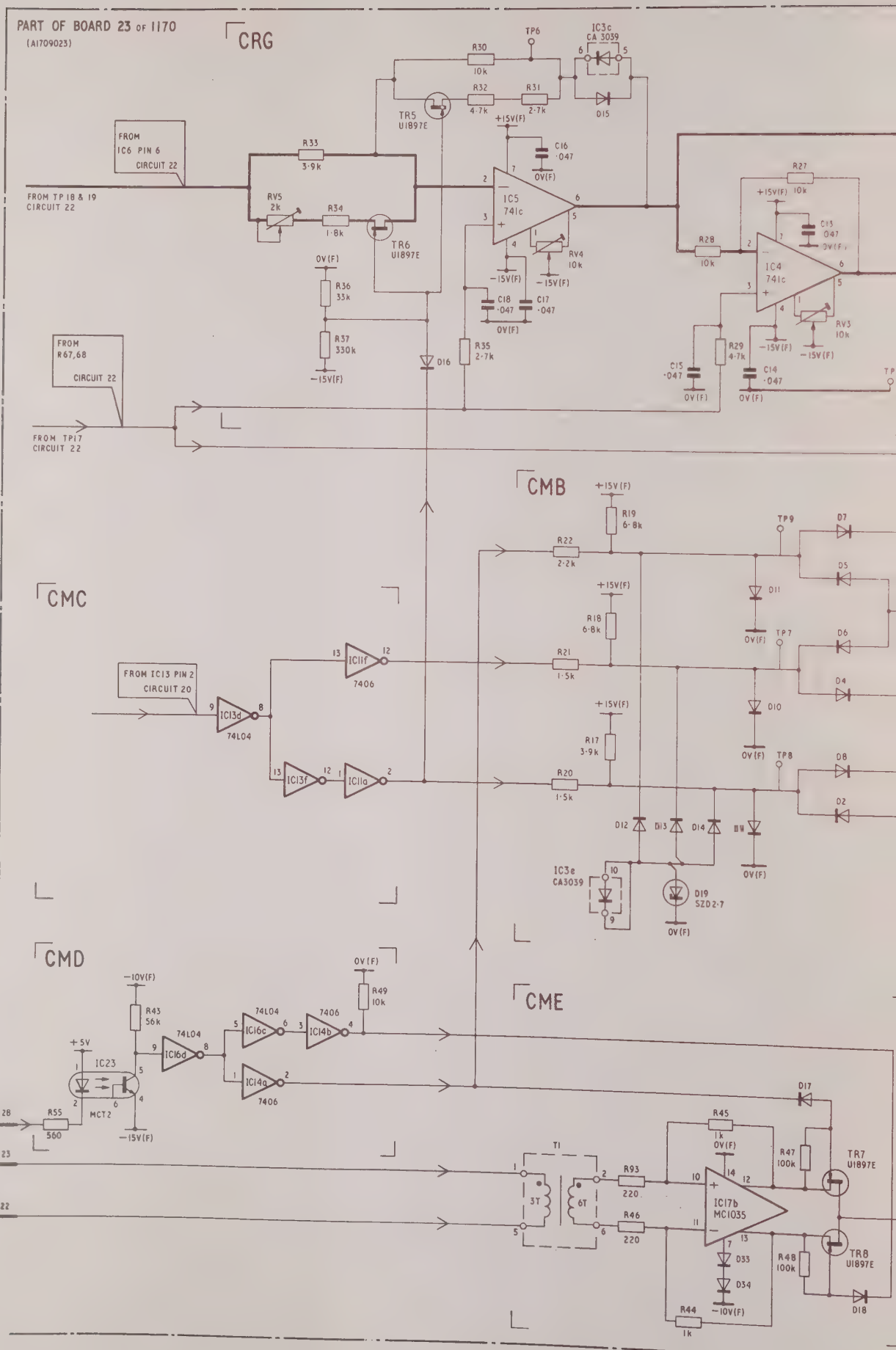
TO R61 SEE CIRCUIT 21

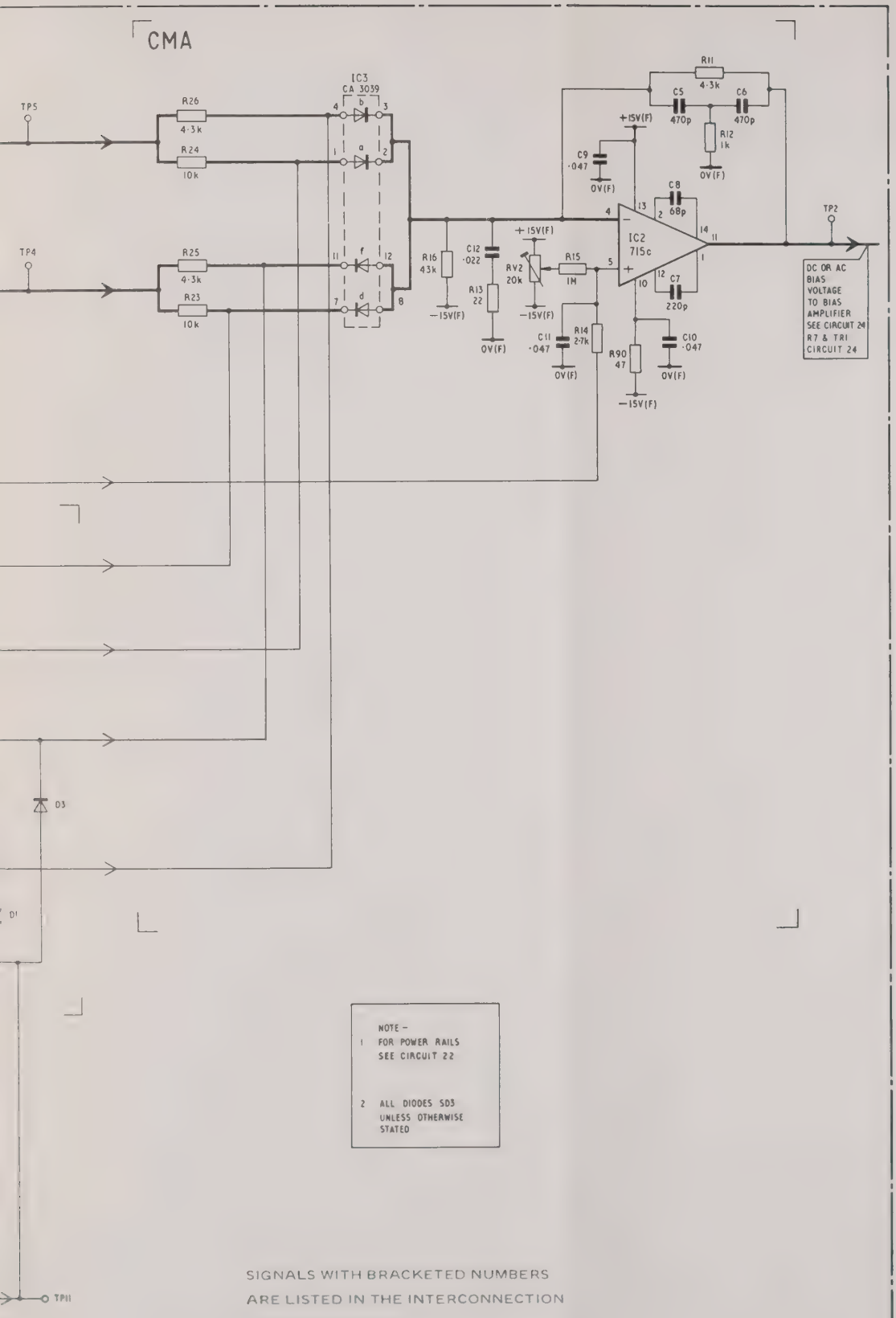
+10·6V REFERENCE

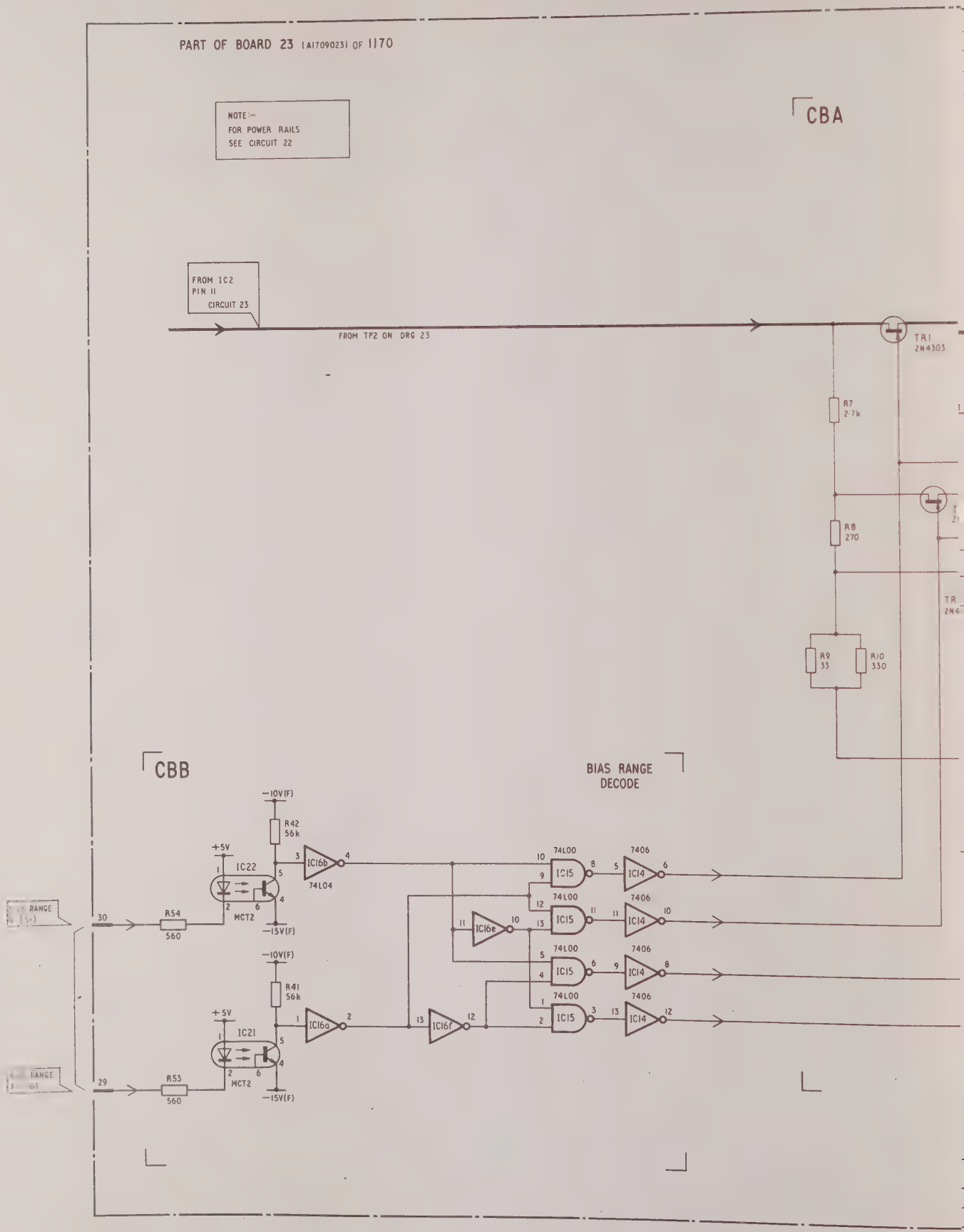
PART OF BOARD 25 (MOTHERBOARD) (AI709025) OF 1170

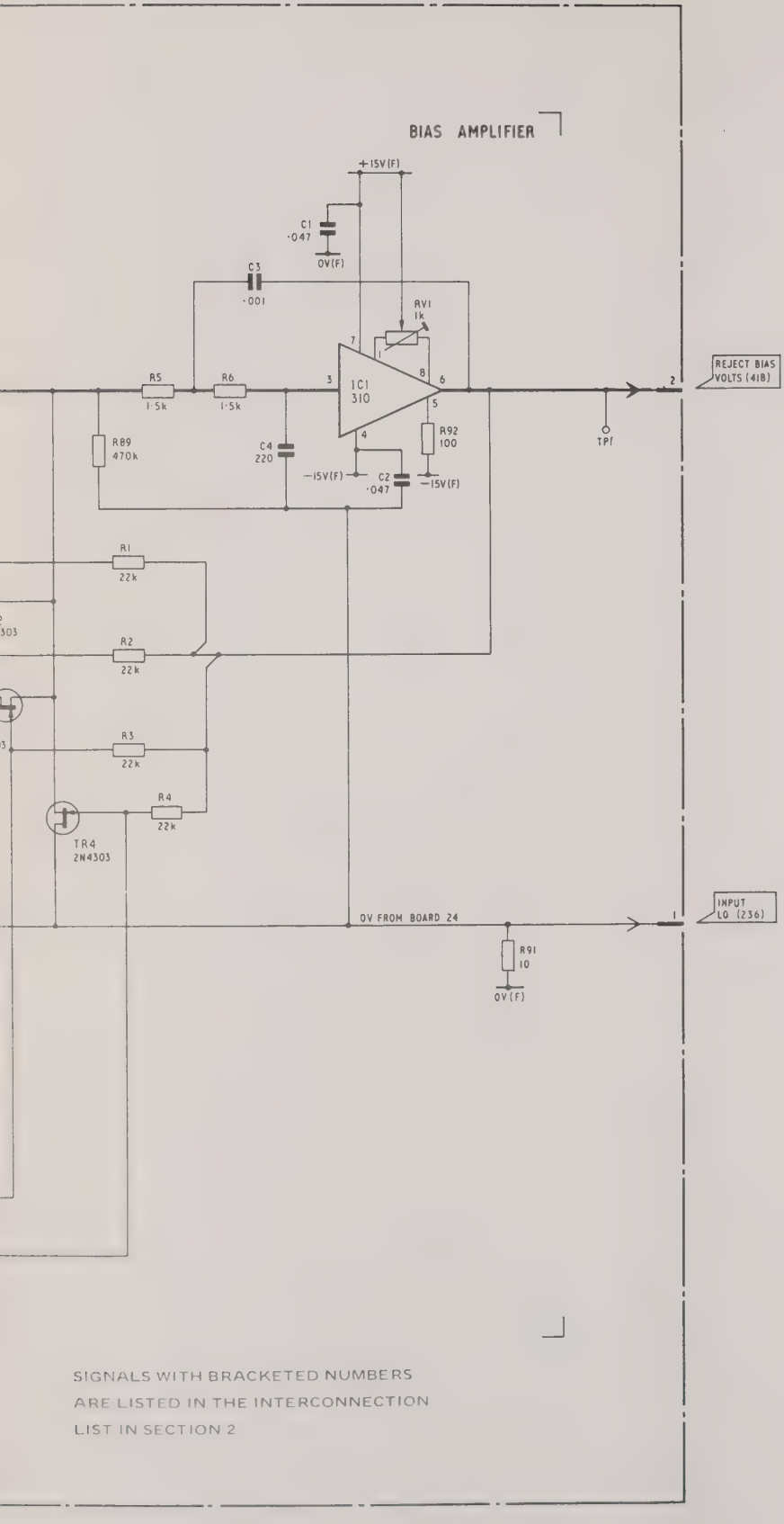


SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

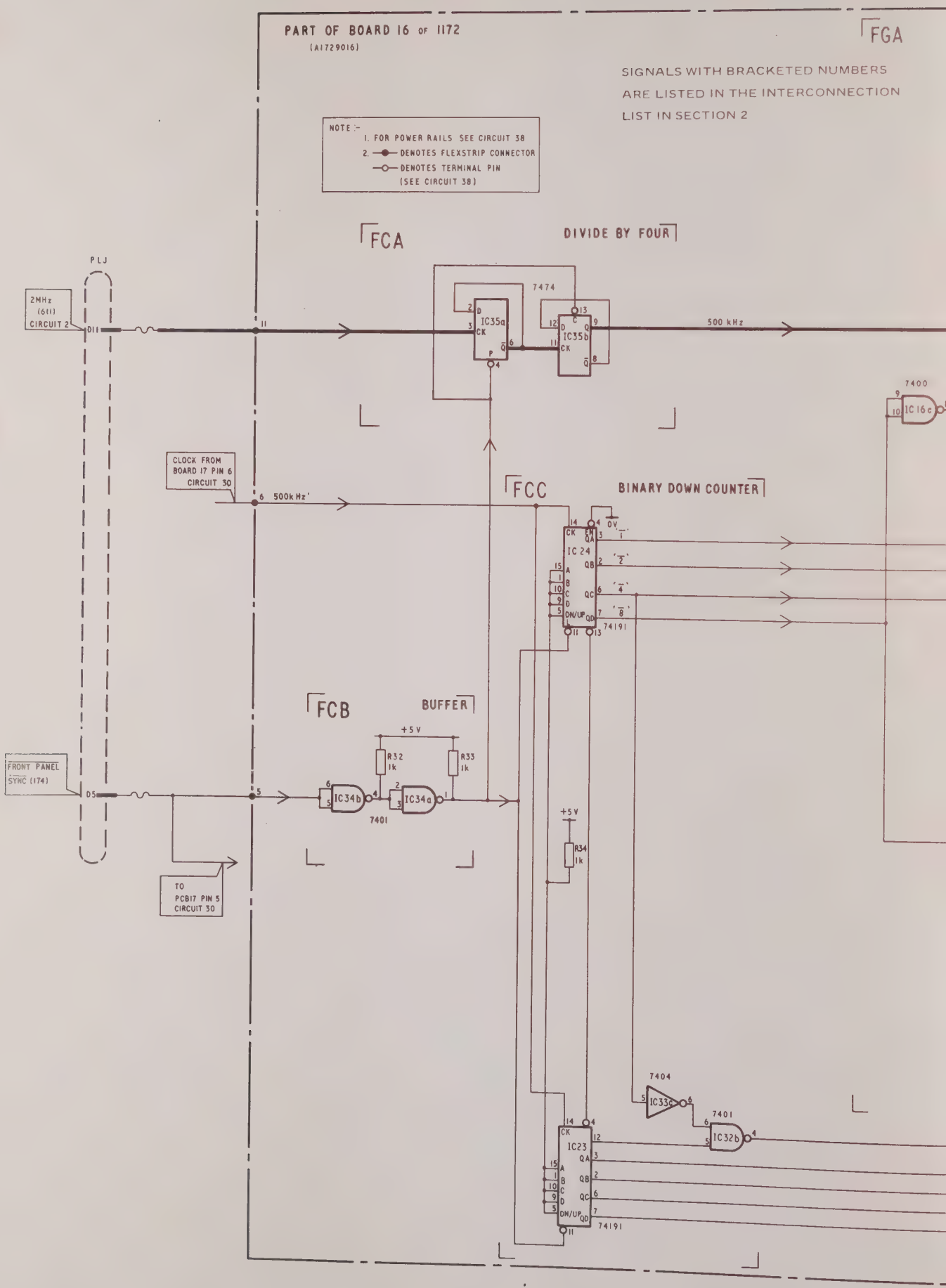

PART OF BOARD 23 OF 1170
(A1709023)
CRG
CMB
CMC
CMD
CME
FROM IC6 PIN 6 CIRCUIT 22
FROM TP 18 & 19 CIRCUIT 22
FROM R67,68 CIRCUIT 22
FROM TP17 CIRCUIT 22
FROM IC13 PIN 2 CIRCUIT 20
TP6
IC3c CA 3039
R30 10k
R32 4·7k
R31 2·7k
D15
TR5 U1897E
+15V(F)
C16 ·047
0V(F)
R33 3·9k
RV5 2k
R34 1·8k
TR6 U1897E
IC5 741c
RV4 10k
-15V(F)
C18 ·047
C17 ·047
R36 33k
R37 330k
R35 2·7k
D16
R27 10k
C13 ·047
IC4 741c
RV3 10k
R28 10k
R29 4·7k
C15 ·047
C14 ·047
R19 6·8k
R22 2·2k
R18 6·8k
R21 1·5k
R17 3·9k
R20 1·5k
TP9
TP7
TP8
D7
D5
D6
D4
D8
D2
D11
D10
D12
D13
D14
IC3e CA3039
D19 SZD2·7
IC11f
IC13d
IC13f
IC11a
7406
74L04
R43 56k
-10V(F)
+5V
IC23
MCT2
R55 560
IC16d
IC16c
IC14b
IC14a
R49 10k
REJ BIAS POLARITY (4:7)
CORRELATOR CARRIER MARK—SPACE (6:2)
CORRELATOR CARRIER MARK—SPACE (6:1)
T1
3T
6T
R93 220
R46 220
IC17b MC1035
R45 1k
R47 100k
R48 100k
R44 1k
D17
D33
D34
TR7 U1897E
TR8 U1897E
D18

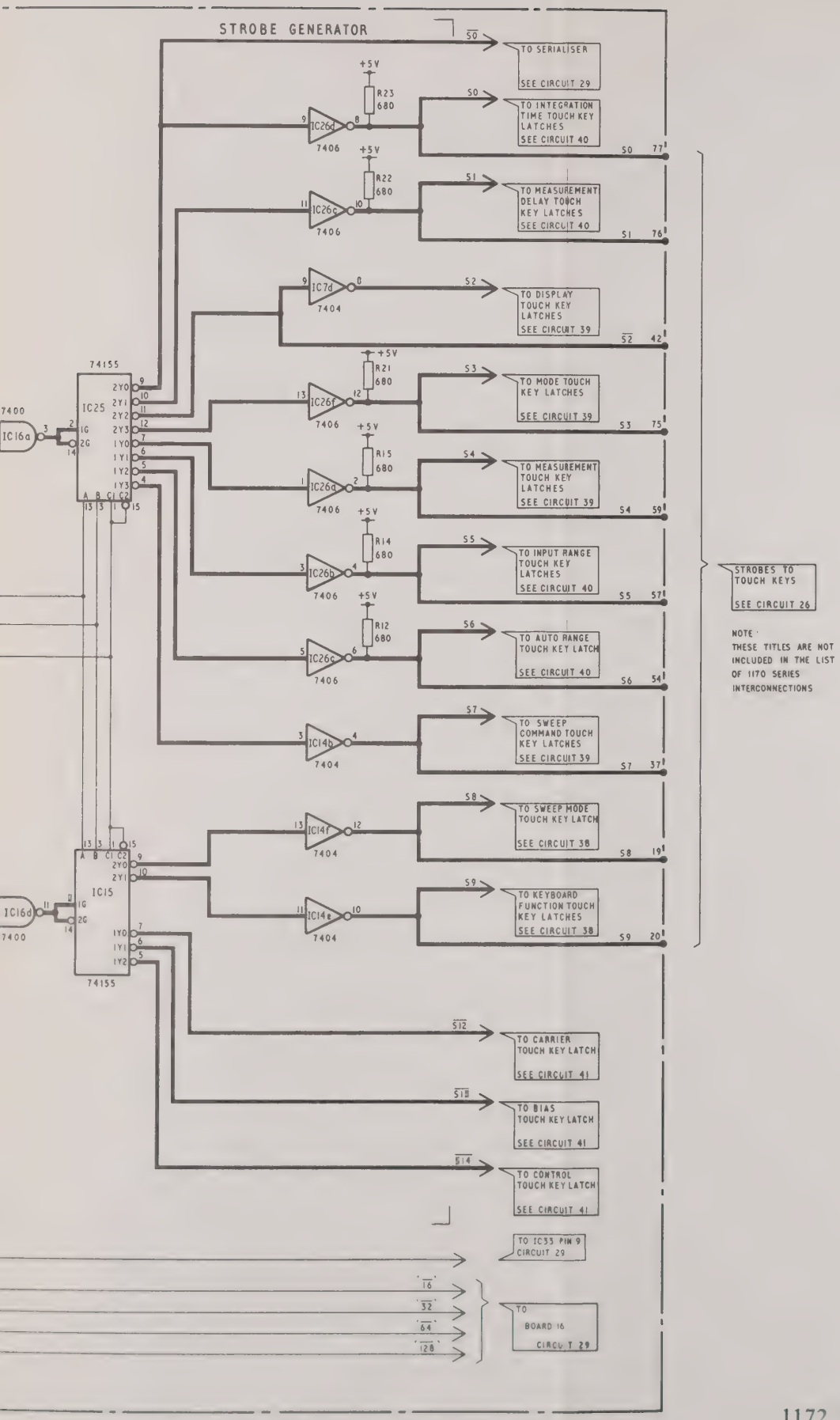

CMA
IC3
CA 3039
TP5
TP4
R26
4·3k
R24
10k
R25
4·3k
R23
10k
R16
43k
C12
·022
R13
22
RV2
20k
R15
1M
C11
·047
R14
2·7k
R90
47
C10
·047
C9
·047
C8
68p
C7
220p
R11
4·3k
C5
470p
C6
470p
R12
1k
+15V(F)
−15V(F)
0V(F)
IC2
715c
TP2
DC OR AC
BIAS
VOLTAGE
TO BIAS
AMPLIFIER
SEE CIRCUIT 24
R7 & TR1
CIRCUIT 24
D3
D1
TP11
NOTE –
1 FOR POWER RAILS SEE CIRCUIT 22
2 ALL DIODES SD3 UNLESS OTHERWISE STATED
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

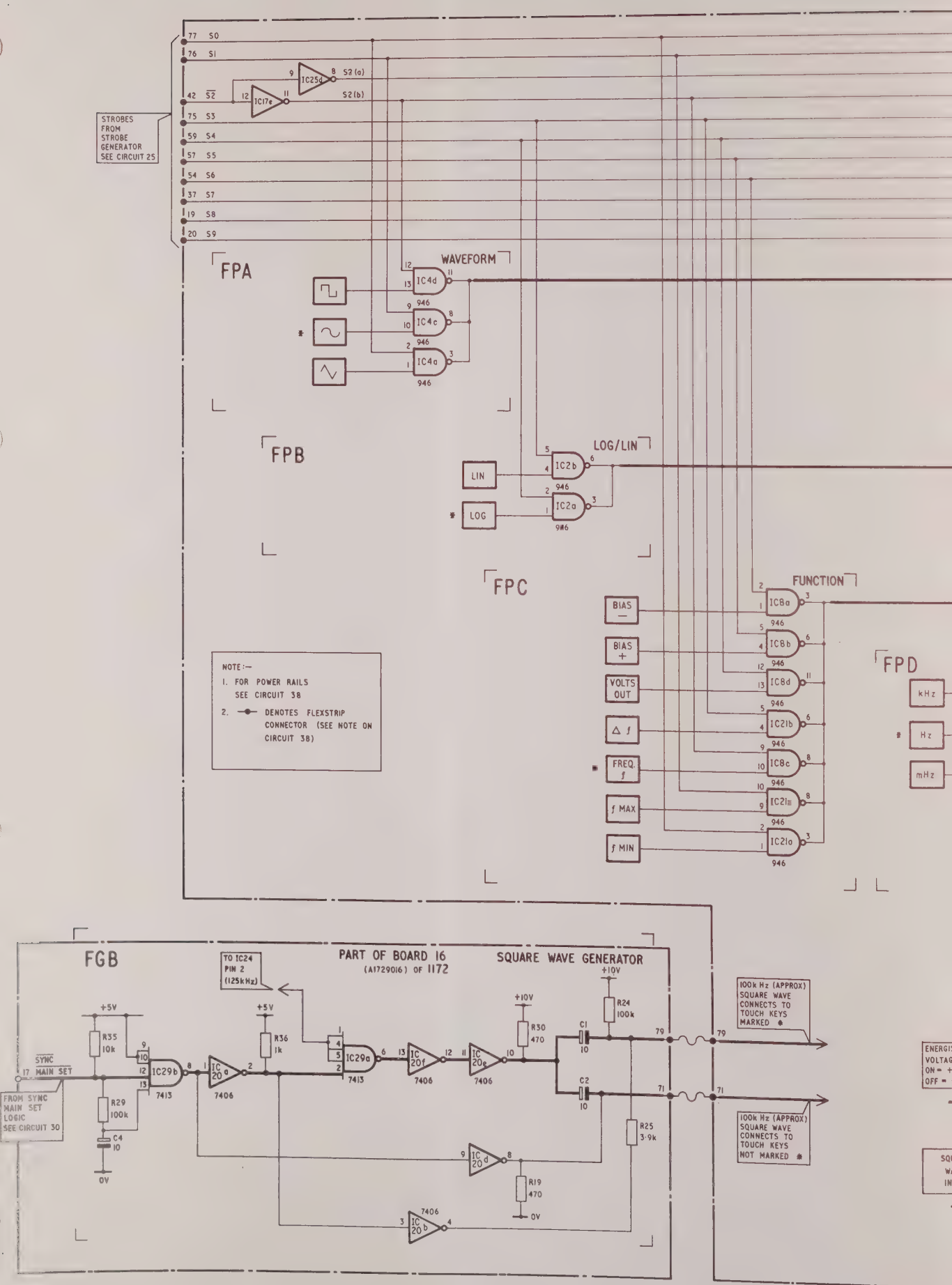

PART OF BOARD 23 (AI709023) OF 1170
NOTE:-
FOR POWER RAILS
SEE CIRCUIT 22
CBA
FROM IC2
PIN 11
CIRCUIT 23
FROM TP2 ON DRG 23
TR1
2N4303
R7
2·7k
R8
270
R9
33
R10
330
CBB
BIAS RANGE
DECODE
-10V(F)
R42
56k
+5V
IC22
IC16b
74L04
MCT2
-15V(F)
R54
560
30
R41
56k
IC21
IC16a
R53
560
29
IC16e
IC16f
74L00
IC15
7406
IC14

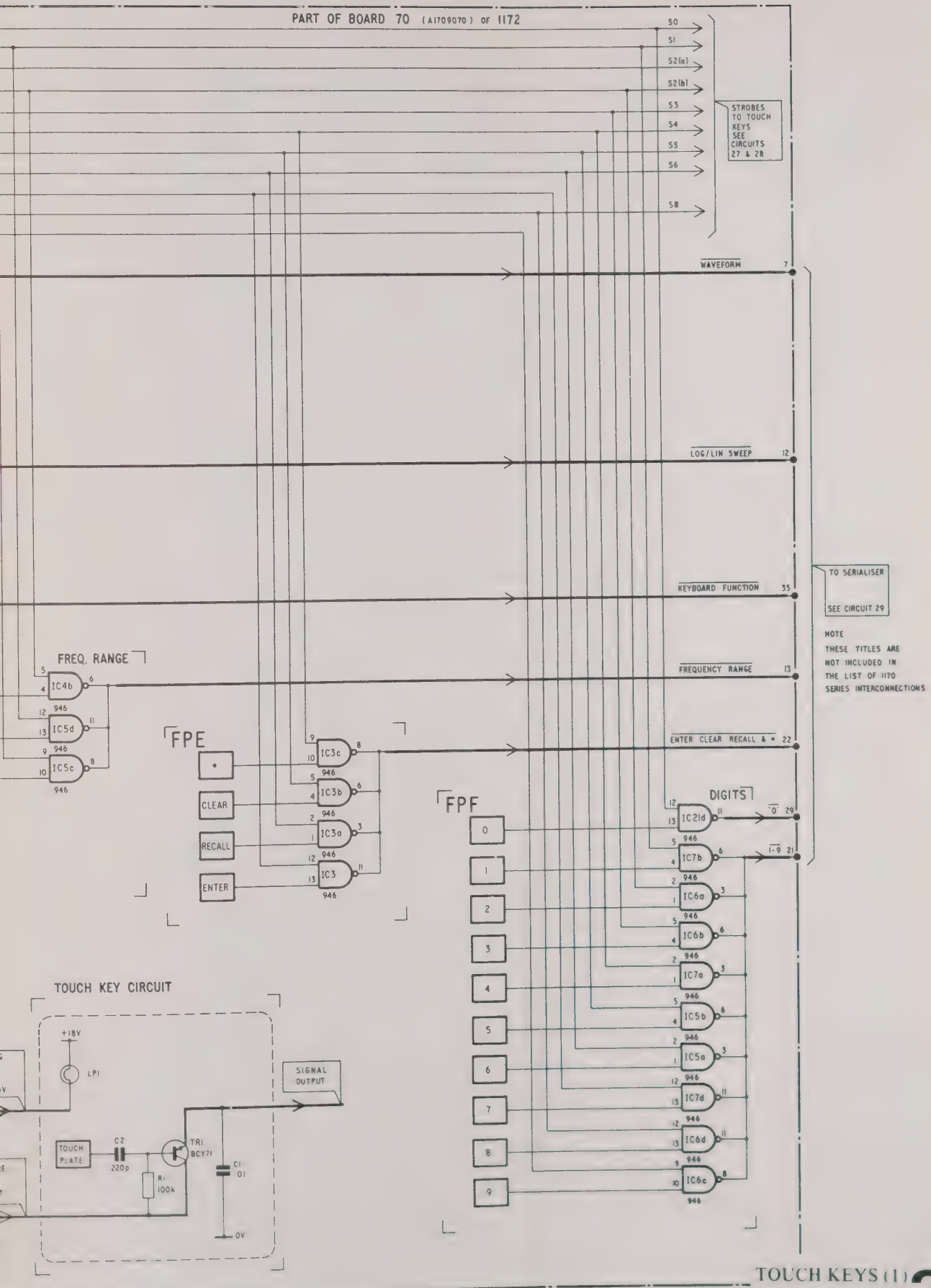


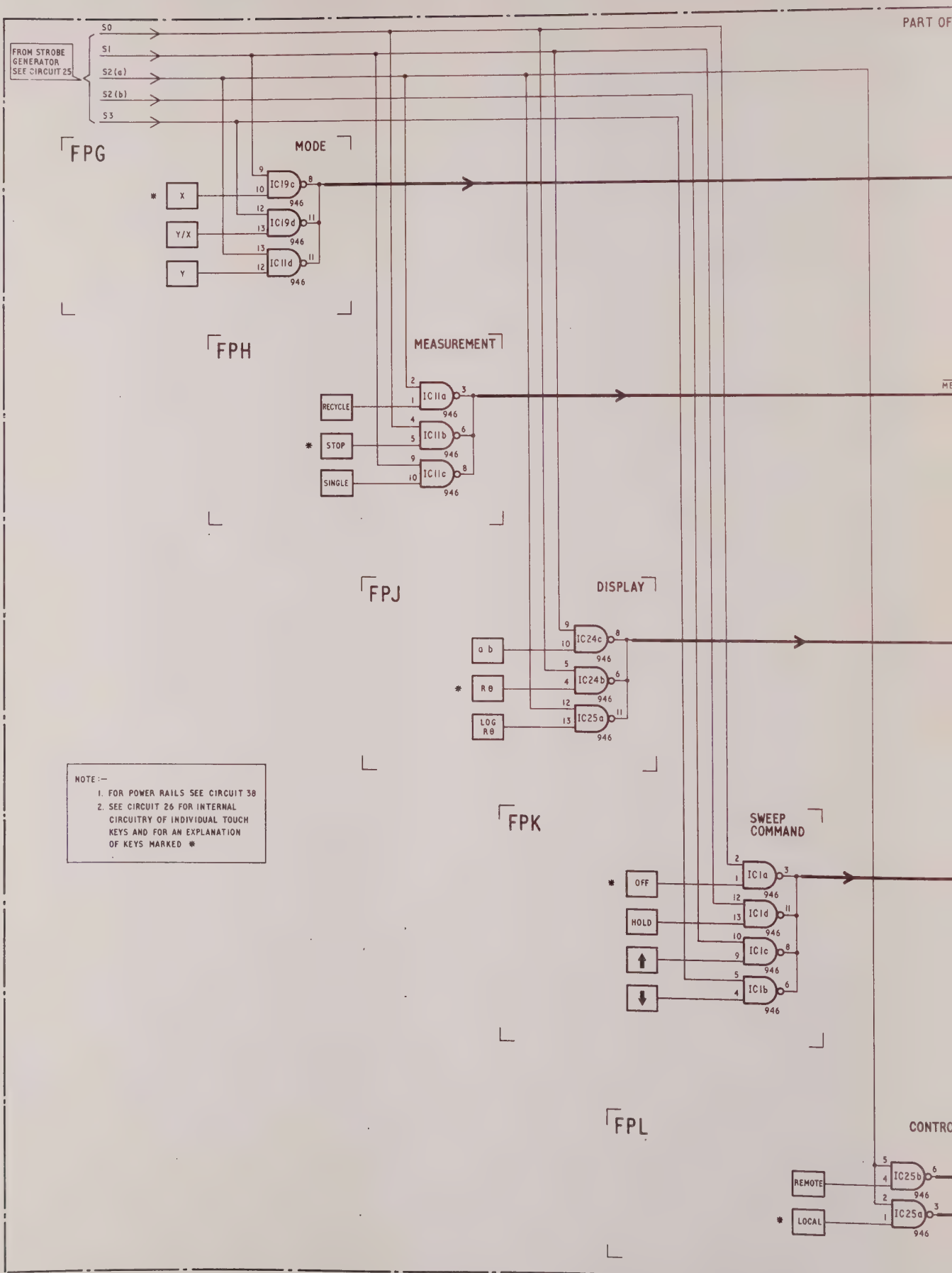
SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2

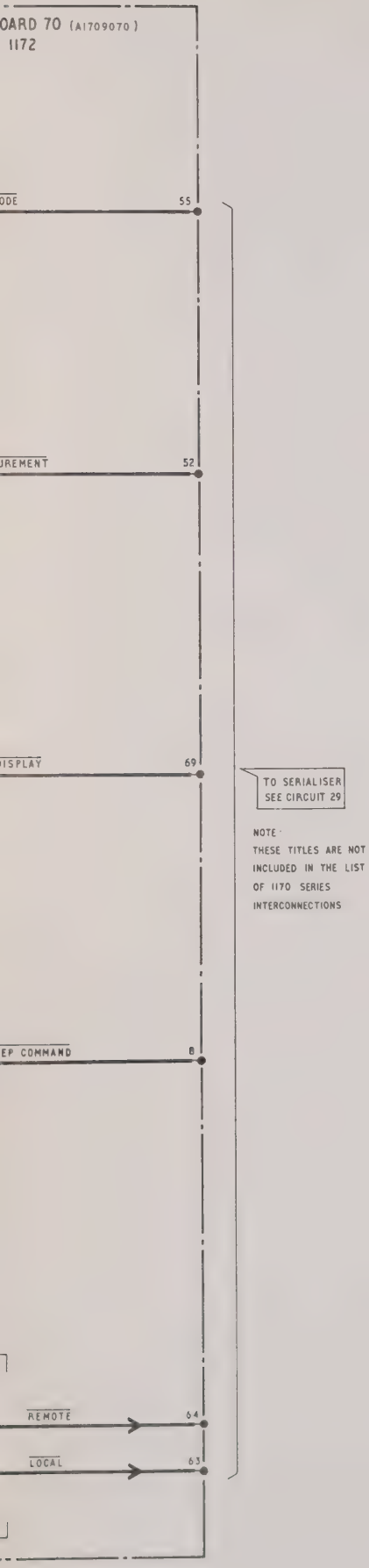

PART OF BOARD 16 OF 1172
(A1729016)
FGA
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2
NOTE :-
1. FOR POWER RAILS SEE CIRCUIT 38
2. DENOTES FLEXSTRIP CONNECTOR
DENOTES TERMINAL PIN (SEE CIRCUIT 38)
FCA
DIVIDE BY FOUR
PLJ
2MHz (611) CIRCUIT 2
D11
7474
IC35a
IC35b
500 kHz
7400
IC 16 c
CLOCK FROM BOARD 17 PIN 6 CIRCUIT 30
6
500k Hz
FCC
BINARY DOWN COUNTER
IC 24
74191
0V
QA
QB
QC
QD
DN/UP
FCB
BUFFER
+5 V
R32 1k
R33 1k
R34 1k
FRONT PANEL SYNC (174)
D5
IC34b
IC34a
7401
TO PCB17 PIN 5 CIRCUIT 30
7404
IC33c
IC32b
IC23
74191

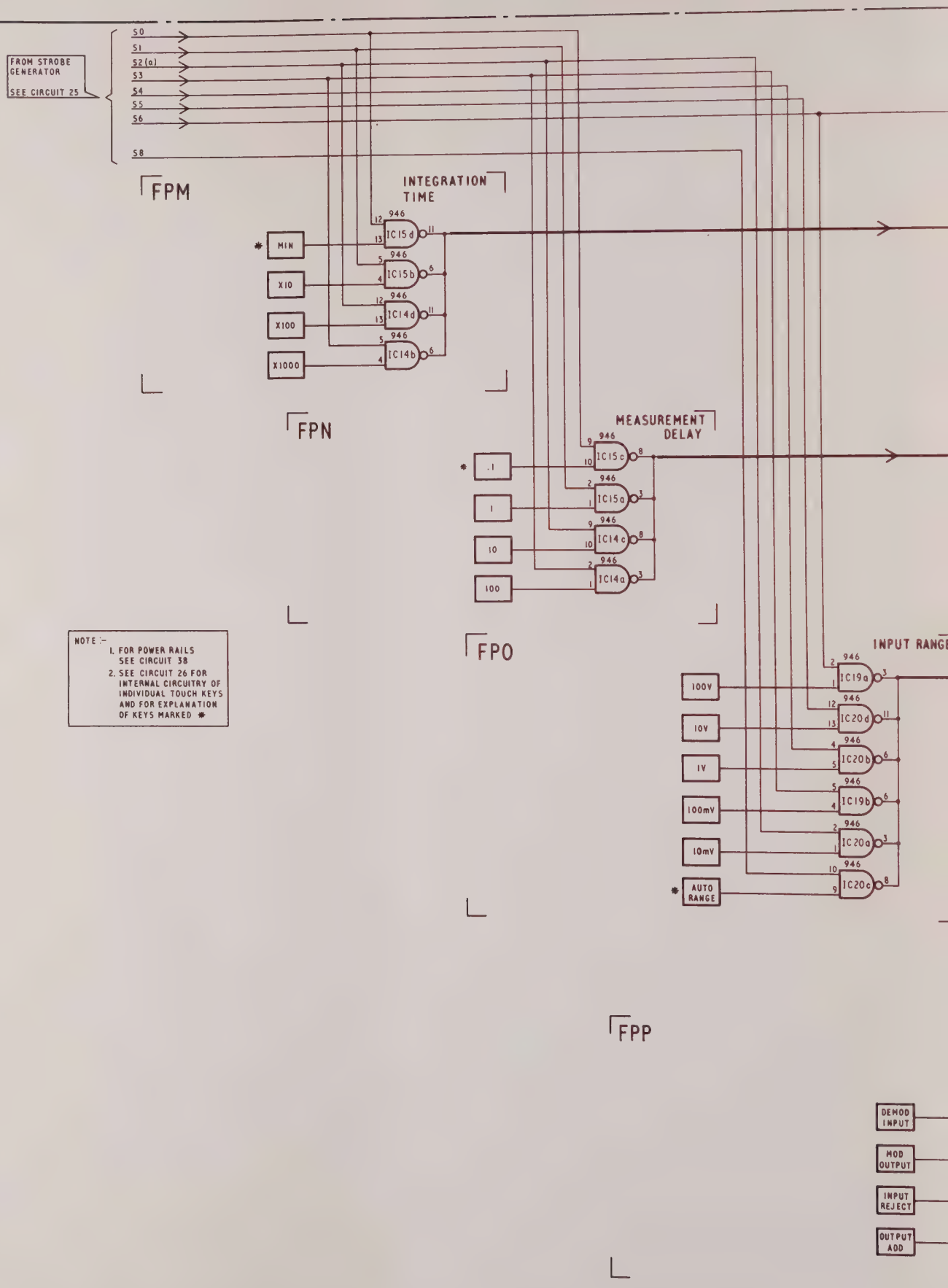

STROBE GENERATOR
S0
TO SERIALISER
SEE CIRCUIT 29
+5V
R23
680
IC26d
7406
S0
TO INTEGRATION TIME TOUCH KEY LATCHES
SEE CIRCUIT 40
S0 77
+5V
R22
680
IC26c
7406
S1
TO MEASUREMENT DELAY TOUCH KEY LATCHES
SEE CIRCUIT 40
S1 76
IC7d
7404
S2
TO DISPLAY TOUCH KEY LATCHES
SEE CIRCUIT 39
S2 42
74155
IC25
+5V
R21
680
IC26f
7406
S3
TO MODE TOUCH KEY LATCHES
SEE CIRCUIT 39
S3 75
7400
IC16a
+5V
R15
680
IC26a
7406
S4
TO MEASUREMENT TOUCH KEY LATCHES
SEE CIRCUIT 39
S4 59
+5V
R14
680
IC26b
7406
S5
TO INPUT RANGE TOUCH KEY LATCHES
SEE CIRCUIT 40
S5 57
+5V
R12
680
IC26c
7406
S6
TO AUTO RANGE TOUCH KEY LATCH
SEE CIRCUIT 40
S6 54
IC14b
7404
S7
TO SWEEP COMMAND TOUCH KEY LATCHES
SEE CIRCUIT 39
S7 37
IC14f
7404
S8
TO SWEEP MODE TOUCH KEY LATCH
SEE CIRCUIT 38
S8 19
IC15
74155
IC16d
7400
IC14e
7404
S9
TO KEYBOARD FUNCTION TOUCH KEY LATCHES
SEE CIRCUIT 38
S9 20
STROBES TO TOUCH KEYS
SEE CIRCUIT 26
NOTE
THESE TITLES ARE NOT INCLUDED IN THE LIST OF 1170 SERIES INTERCONNECTIONS
S12
TO CARRIER TOUCH KEY LATCH
SEE CIRCUIT 41
S11
TO BIAS TOUCH KEY LATCH
SEE CIRCUIT 41
S14
TO CONTROL TOUCH KEY LATCH
SEE CIRCUIT 41
TO IC33 PIN 9
CIRCUIT 29
16
32
64
128
TO
BOARD 16
CIRCUIT 29

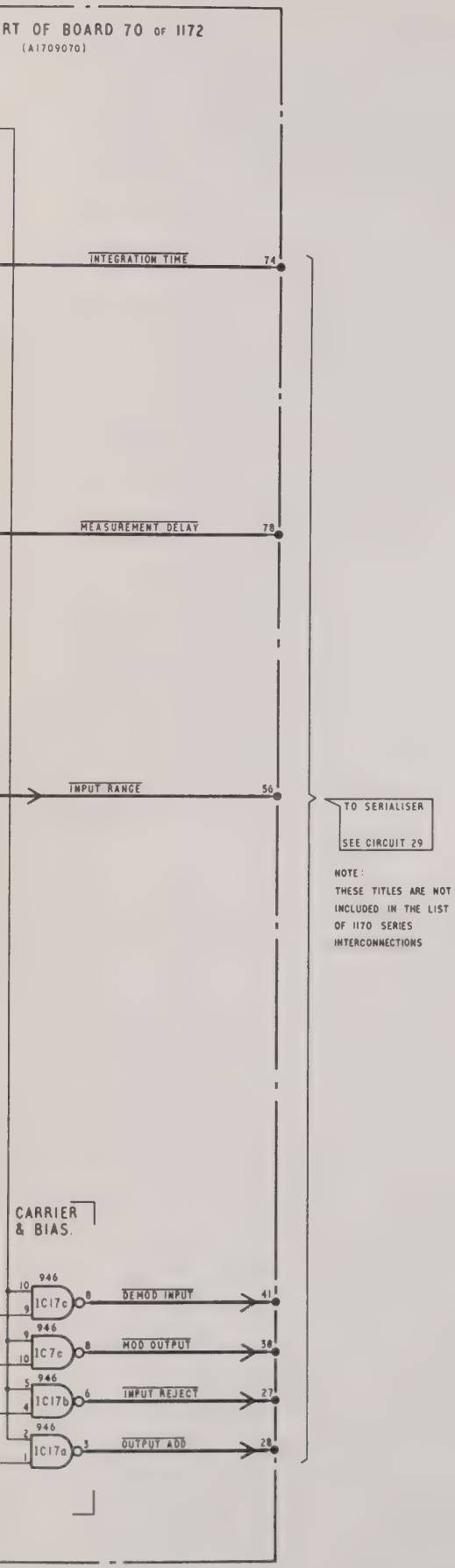

STROBES FROM STROBE GENERATOR SEE CIRCUIT 25
77 S0
76 S1
42 S2
75 S3
59 S4
57 S5
54 S6
37 S7
19 S8
20 S9
IC25d
IC17e
S2(a)
S2(b)
FPA
WAVEFORM
IC4d
IC4c
IC4a
946
FPB
LOG/LIN
LIN
LOG
IC2b
IC2a
FPC
FUNCTION
BIAS —
BIAS +
VOLTS OUT
Δ f
FREQ. f
f MAX
f MIN
IC8a
IC8b
IC8d
IC21b
IC8c
IC21a
NOTE:—
1. FOR POWER RAILS SEE CIRCUIT 38
2. DENOTES FLEXSTRIP CONNECTOR (SEE NOTE ON CIRCUIT 38)
FPD
kHz
Hz
mHz
FGB
PART OF BOARD 16 (A1729016) OF 1172
SQUARE WAVE GENERATOR
TO IC24 PIN 2 (125kHz)
+5V
+10V
R35 10k
R36 1k
R24 100k
R30 470
R29 100k
R25 3·9k
R19 470
C1 10
C2 10
C4 10
0V
SYNC MAIN SET
17
FROM SYNC MAIN SET LOGIC SEE CIRCUIT 30
IC29b
IC29a
IC20a
IC20b
IC20d
IC20e
IC20f
7413
7406
100k Hz (APPROX) SQUARE WAVE CONNECTS TO TOUCH KEYS MARKED *
100k Hz (APPROX) SQUARE WAVE CONNECTS TO TOUCH KEYS NOT MARKED *
79
71

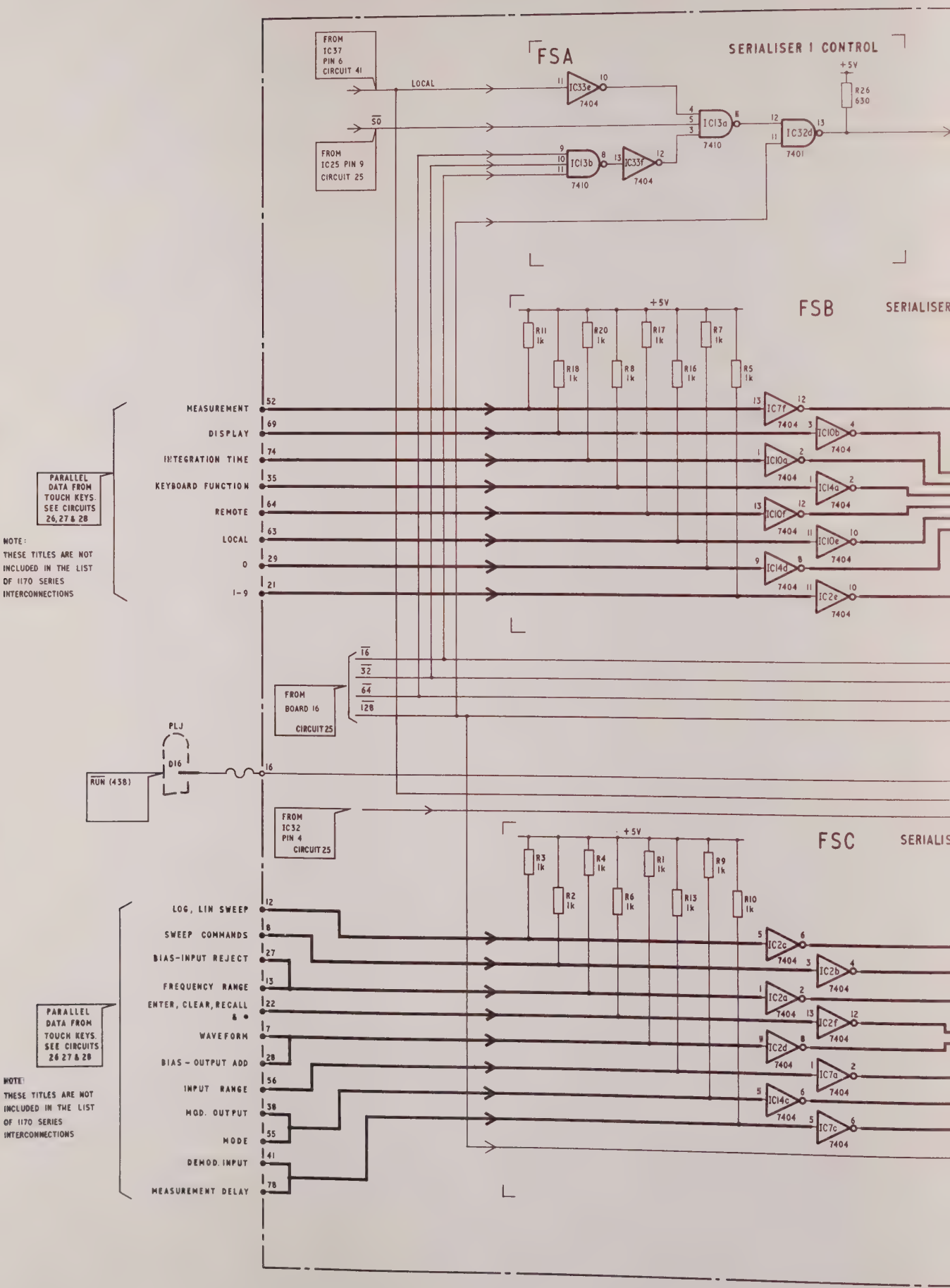

PART OF BOARD 70 (A1709070) OF 1172
S0
S1
S2(a)
S2(b)
S3
S4
S5
S6
S11
STROBES TO TOUCH KEYS SEE CIRCUITS 27 & 28
WAVEFORM 7
LOG/LIN SWEEP 12
KEYBOARD FUNCTION 35
FREQUENCY RANGE 13
ENTER CLEAR RECALL & • 22
TO SERIALISER
SEE CIRCUIT 29
NOTE
THESE TITLES ARE NOT INCLUDED IN THE LIST OF 1170 SERIES INTERCONNECTIONS
FREQ. RANGE
IC4b
IC5d
IC5c
946
FPE
•
CLEAR
RECALL
ENTER
IC3c
IC3b
IC3a
IC3
FPF
0
1
2
3
4
5
6
7
8
9
DIGITS
IC21d
IC7b
IC6a
IC6b
IC7a
IC5b
IC5a
IC7d
IC6d
IC6c
'0' 29
'1-9' 21
TOUCH KEY CIRCUIT
+18V
LP1
SIGNAL OUTPUT
TOUCH PLATE
C2
220p
TR1
BCY71
R1
100k
C1
01
0V

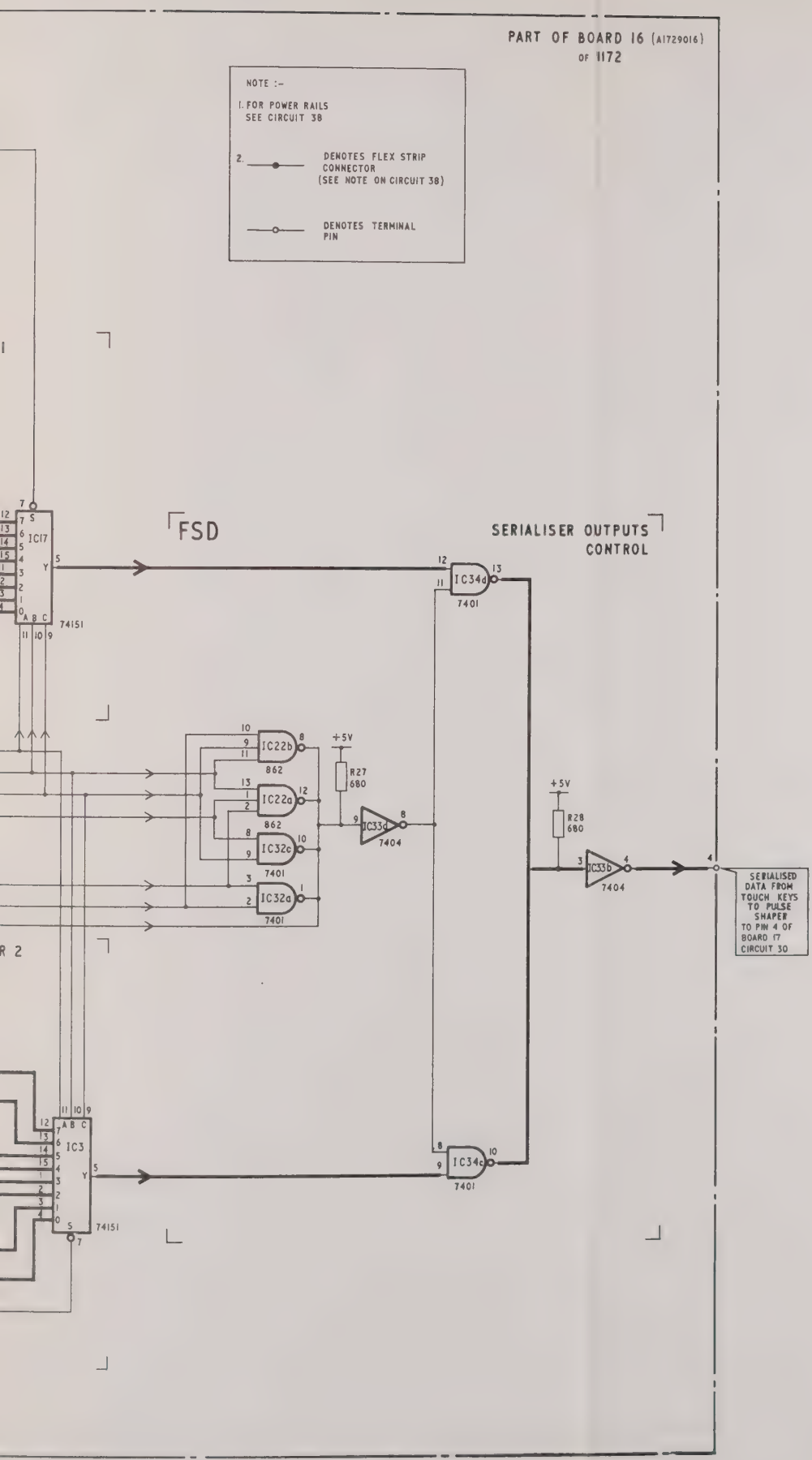

PART OF
FROM STROBE GENERATOR SEE CIRCUIT 25
S0
S1
S2(a)
S2(b)
S3
FPG
MODE
X
Y/X
Y
IC19c
IC19d
IC11d
946
FPH
MEASUREMENT
RECYCLE
STOP
SINGLE
IC11a
IC11b
IC11c
946
FPJ
DISPLAY
a b
R θ
LOG R θ
IC24c
IC24b
IC25a
946
NOTE :-
1. FOR POWER RAILS SEE CIRCUIT 38
2. SEE CIRCUIT 26 FOR INTERNAL CIRCUITRY OF INDIVIDUAL TOUCH KEYS AND FOR AN EXPLANATION OF KEYS MARKED *
FPK
SWEEP COMMAND
OFF
HOLD
IC1a
IC1d
IC1c
IC1b
946
FPL
CONTRO
REMOTE
LOCAL
IC25b
IC25a
946

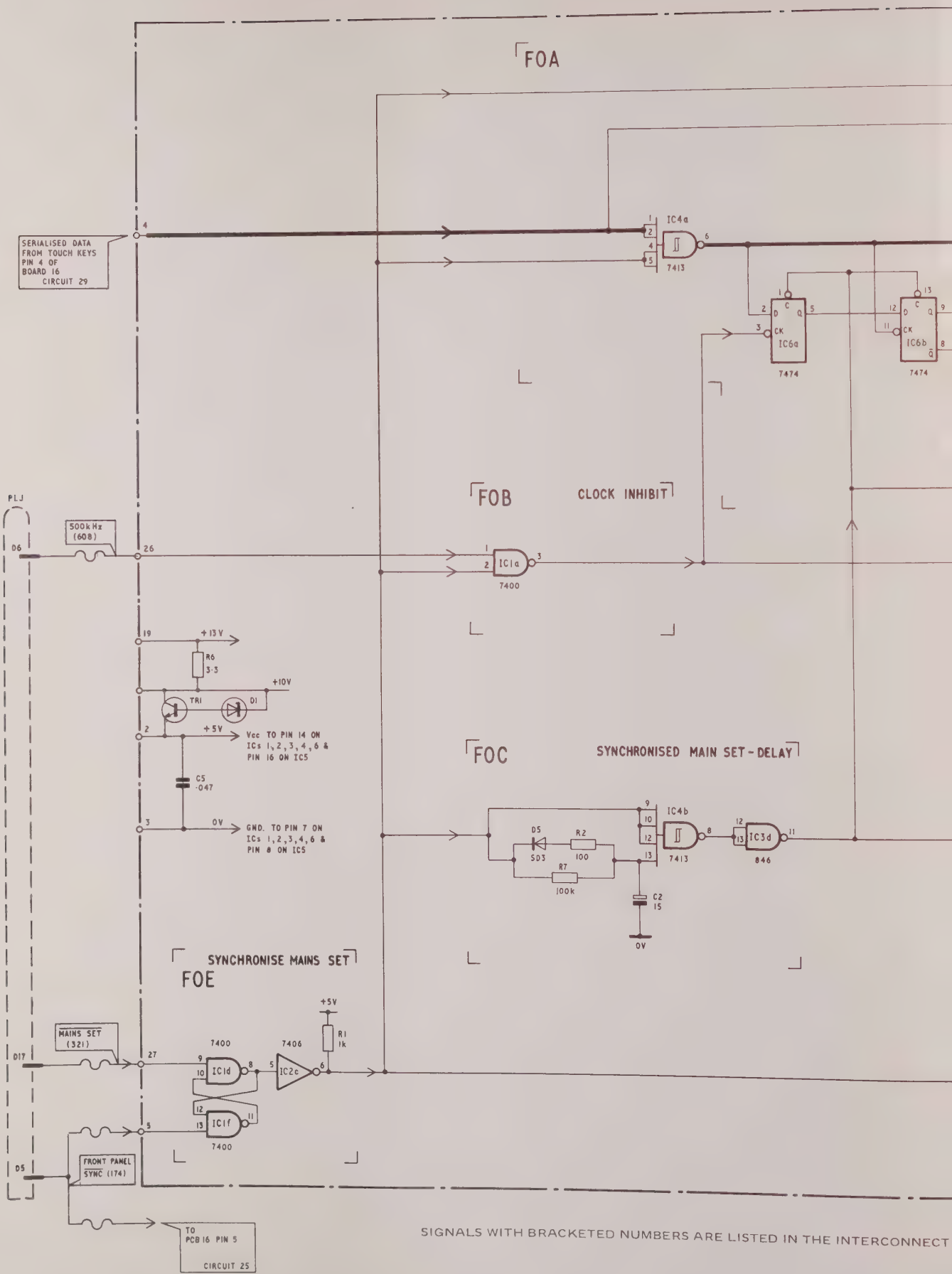

OARD 70 (A1709070)
1172
ODE
55
UREMENT
52
ISPLAY
69
TO SERIALISER
SEE CIRCUIT 29
NOTE
THESE TITLES ARE NOT
INCLUDED IN THE LIST
OF 1170 SERIES
INTERCONNECTIONS
EP COMMAND
8
REMOTE
64
LOCAL
63


FROM STROBE GENERATOR
SEE CIRCUIT 25
S0
S1
S2(a)
S3
S4
S5
S6
S8
FPM
INTEGRATION TIME
946
IC15d
IC15b
IC14d
IC14b
MIN
X10
X100
X1000
FPN
MEASUREMENT DELAY
IC15c
IC15a
IC14c
IC14a
.1
1
10
100
FPO
INPUT RANGE
IC19a
IC20d
IC20b
IC19b
IC20a
IC20c
100V
10V
1V
100mV
10mV
AUTO RANGE
FPP
DEMOD INPUT
MOD OUTPUT
INPUT REJECT
OUTPUT ADD
NOTE :-
1. FOR POWER RAILS SEE CIRCUIT 38
2. SEE CIRCUIT 26 FOR INTERNAL CIRCUITRY OF INDIVIDUAL TOUCH KEYS AND FOR EXPLANATION OF KEYS MARKED *

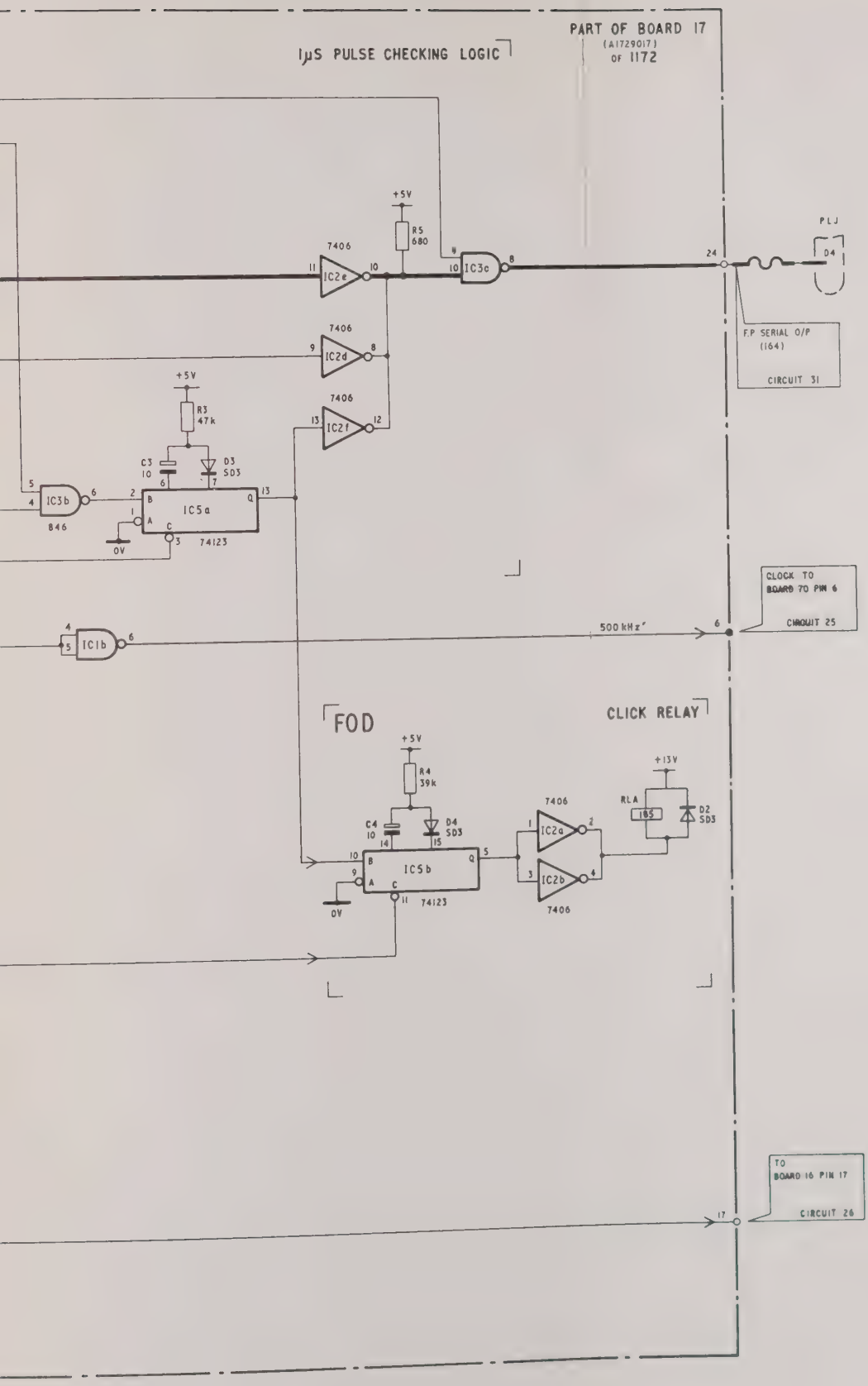

RT OF BOARD 70 OF 1172
(A1709070)
INTEGRATION TIME
74
MEASUREMENT DELAY
78
INPUT RANGE
56
TO SERIALISER
SEE CIRCUIT 29
NOTE:
THESE TITLES ARE NOT
INCLUDED IN THE LIST
OF 1170 SERIES
INTERCONNECTIONS
CARRIER
& BIAS.
946
1C17c
DEMOD INPUT
41
946
1C7c
MOD OUTPUT
38
946
1C17b
INPUT REJECT
27
946
1C17a
OUTPUT ADD
28


FSA
SERIALISER I CONTROL
FROM IC37 PIN 6 CIRCUIT 41
LOCAL
S0
FROM IC25 PIN 9 CIRCUIT 25
IC33e
IC13a
IC32d
IC13b
IC33f
7404
7410
7401
+5V
R26 630
FSB
SERIALISER
R11 1k
R20 1k
R17 1k
R7 1k
R18 1k
R8 1k
R16 1k
R5 1k
MEASUREMENT
DISPLAY
INTEGRATION TIME
KEYBOARD FUNCTION
REMOTE
LOCAL
0
1-9
PARALLEL DATA FROM TOUCH KEYS. SEE CIRCUITS 26,27 & 28
NOTE: THESE TITLES ARE NOT INCLUDED IN THE LIST OF 1170 SERIES INTERCONNECTIONS
IC7f
IC10b
IC10a
IC14a
IC10f
IC10e
IC14d
IC2e
FROM BOARD 16 CIRCUIT 25
PLJ
D16
RUN (438)
FROM IC32 PIN 4 CIRCUIT 25
FSC
SERIALIS
R3 1k
R4 1k
R1 1k
R9 1k
R2 1k
R6 1k
R13 1k
R10 1k
LOG, LIN SWEEP
SWEEP COMMANDS
BIAS-INPUT REJECT
FREQUENCY RANGE
ENTER, CLEAR, RECALL & •
WAVEFORM
BIAS - OUTPUT ADD
INPUT RANGE
MOD. OUTPUT
MODE
DEMOD. INPUT
MEASUREMENT DELAY
PARALLEL DATA FROM TOUCH KEYS. SEE CIRCUITS 26 27 & 28
NOTE: THESE TITLES ARE NOT INCLUDED IN THE LIST OF 1170 SERIES INTERCONNECTIONS
IC2c
IC2b
IC2a
IC2f
IC2d
IC7a
IC14c
IC7c

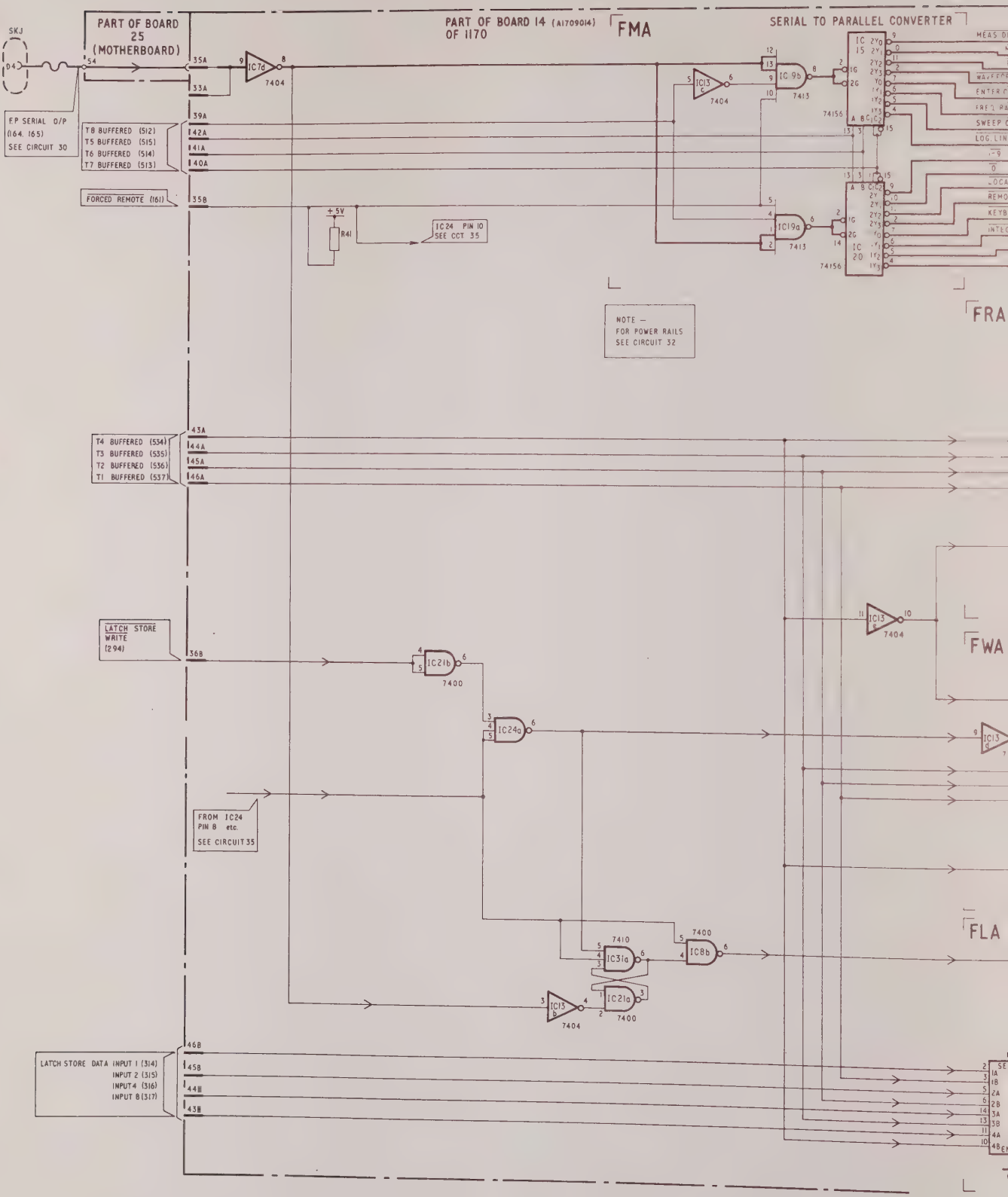

PART OF BOARD 16 (A1729016)
OF 1172
NOTE :-
1. FOR POWER RAILS SEE CIRCUIT 38
2. DENOTES FLEX STRIP CONNECTOR (SEE NOTE ON CIRCUIT 38)
DENOTES TERMINAL PIN
FSD
SERIALISER OUTPUTS CONTROL
IC17
74151
IC34d
7401
IC22b
862
IC22a
862
IC32c
7401
IC32a
7401
+5V
R27
680
IC33c
7404
+5V
R28
680
IC33b
7404
SERIALISED DATA FROM TOUCH KEYS TO PULSE SHAPER TO PIN 4 OF BOARD 17 CIRCUIT 30
IC34c
7401
IC3
74151



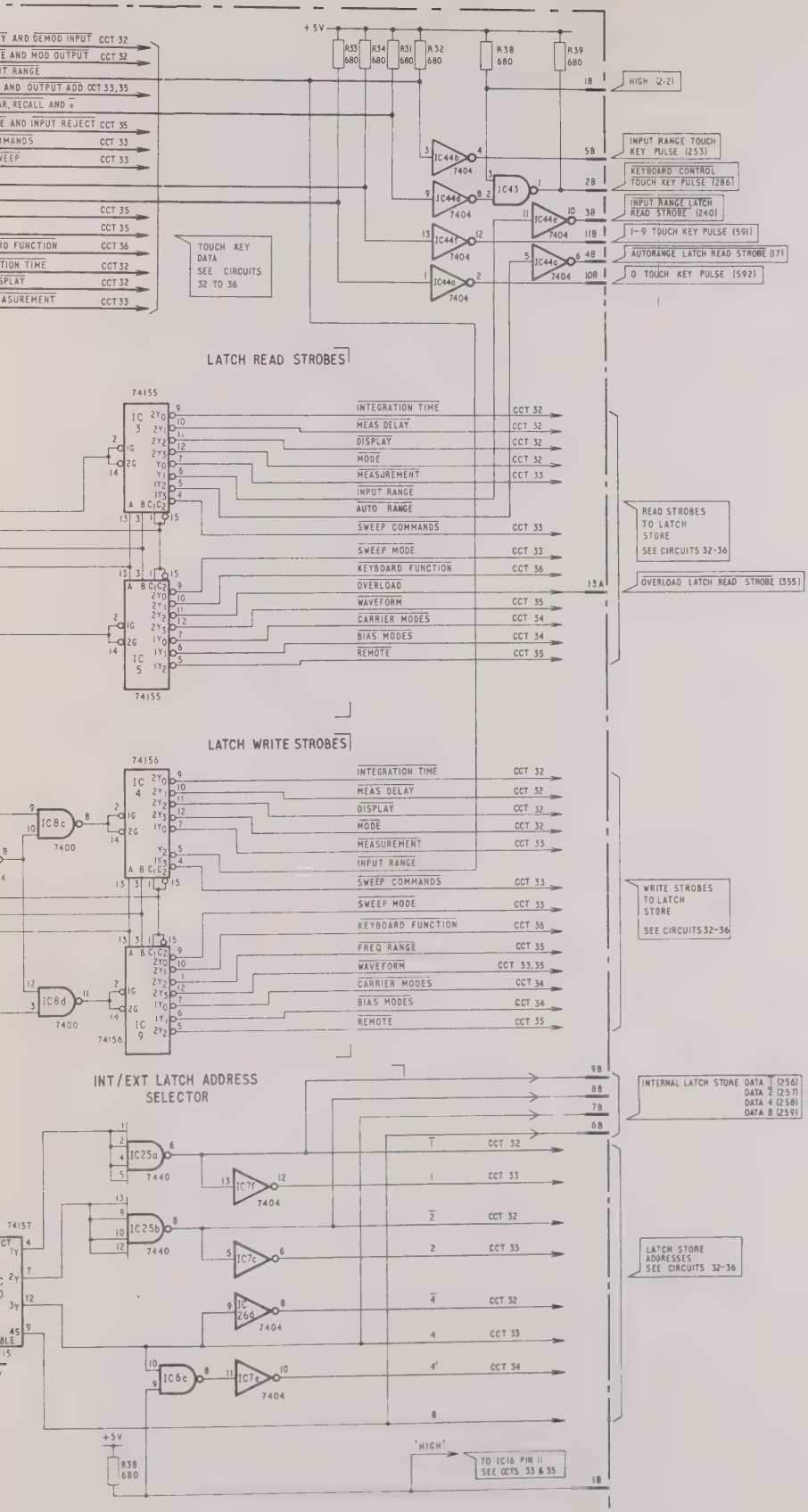
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECT



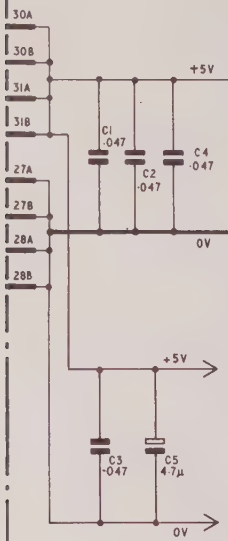
N LIST IN SECTION 2



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


+5V
R33 680
R34 680
R31 680
R32 680
R38 680
R39 680
1B HIGH (2.2)
IC44b 7404
5B INPUT RANGE TOUCH KEY PULSE (253)
IC43
2B KEYBOARD CONTROL TOUCH KEY PULSE (286)
IC44d 7404
3B INPUT RANGE LATCH READ STROBE (240)
IC44e 7404
11B 1-9 TOUCH KEY PULSE (591)
IC44f 7404
4B AUTORANGE LATCH READ STROBE (17)
IC44c 7404
10B 0 TOUCH KEY PULSE (592)
IC44a 7404
TOUCH KEY DATA SEE CIRCUITS 32 TO 36
LATCH READ STROBES
74155
IC 3
INTEGRATION TIME CCT 32
MEAS DELAY CCT 32
DISPLAY CCT 32
MODE CCT 32
MEASUREMENT CCT 33
INPUT RANGE
AUTO RANGE
SWEEP COMMANDS CCT 33
SWEEP MODE CCT 33
KEYBOARD FUNCTION CCT 36
OVERLOAD
WAVEFORM CCT 35
CARRIER MODES CCT 34
BIAS MODES CCT 34
REMOTE CCT 35
IC 5
74155
READ STROBES TO LATCH STORE SEE CIRCUITS 32-36
13A OVERLOAD LATCH READ STROBE (355)
LATCH WRITE STROBES
74156
IC 4
INTEGRATION TIME CCT 32
MEAS DELAY CCT 32
DISPLAY CCT 32
MODE CCT 32
MEASUREMENT CCT 33
INPUT RANGE
SWEEP COMMANDS CCT 33
SWEEP MODE CCT 33
KEYBOARD FUNCTION CCT 36
FREQ RANGE CCT 35
WAVEFORM CCT 33,35
CARRIER MODES CCT 34
BIAS MODES CCT 34
REMOTE CCT 35
IC 9
74156
IC8c 7400
IC8d 7400
WRITE STROBES TO LATCH STORE SEE CIRCUITS 32-36
INT/EXT LATCH ADDRESS SELECTOR
9B
8B
7B
6B
INTERNAL LATCH STORE DATA 1 (256) DATA 2 (257) DATA 4 (258) DATA 8 (259)
IC25a 7440
IC7f 7404
1 CCT 32
1 CCT 33
IC25b 7440
IC7c 7404
2 CCT 32
2 CCT 33
IC 26d 7404
4 CCT 32
4 CCT 33
IC6c
IC7e 7404
4' CCT 34
8
LATCH STORE ADDRESSES SEE CIRCUITS 32-36
74157
+5V
R38 680
'HIGH'
TO IC16 PIN 11 SEE CCTS 33 & 35
1B

PART OF BOARD 14 OF 1170
(A1709014)



FLB

FROM IC3 PIN 9 CIRCUIT 31

FROM IC25 PIN 6 CIRCUIT 31

FROM IC25 PIN 8 CIRCUIT 31

FROM IC4 PIN 9 CIRCUIT 31

FROM IC20 PIN 6 CIRCUIT 31

FLC

FROM IC3 PIN 10 CIRCUIT 31

FROM IC25 PIN 6 CIRCUIT 31

FROM IC25 PIN 8 CIRCUIT 31

FROM IC4 PIN 10 CIRCUIT 31

FROM IC26 PIN 8 CIRCUIT 31

FROM IC15 PIN 9 CIRCUIT 31

+5V

R26 680

FLD

FROM IC3 PIN 11 CIRCUIT 31

FROM IC25 PIN 6 CIRCUIT 31

FROM IC25 PIN 8 CIRCUIT 31

FROM IC4 PIN 11 CIRCUIT 31

FROM IC20 PIN 5 CIRCUIT 31

FLE

FROM IC3 PIN 12 CIRCUIT 31

FROM IC25 PIN 6 CIRCUIT 31

FROM IC25 PIN 8 CIRCUIT 31

FROM IC4 PIN 12 CIRCUIT 31

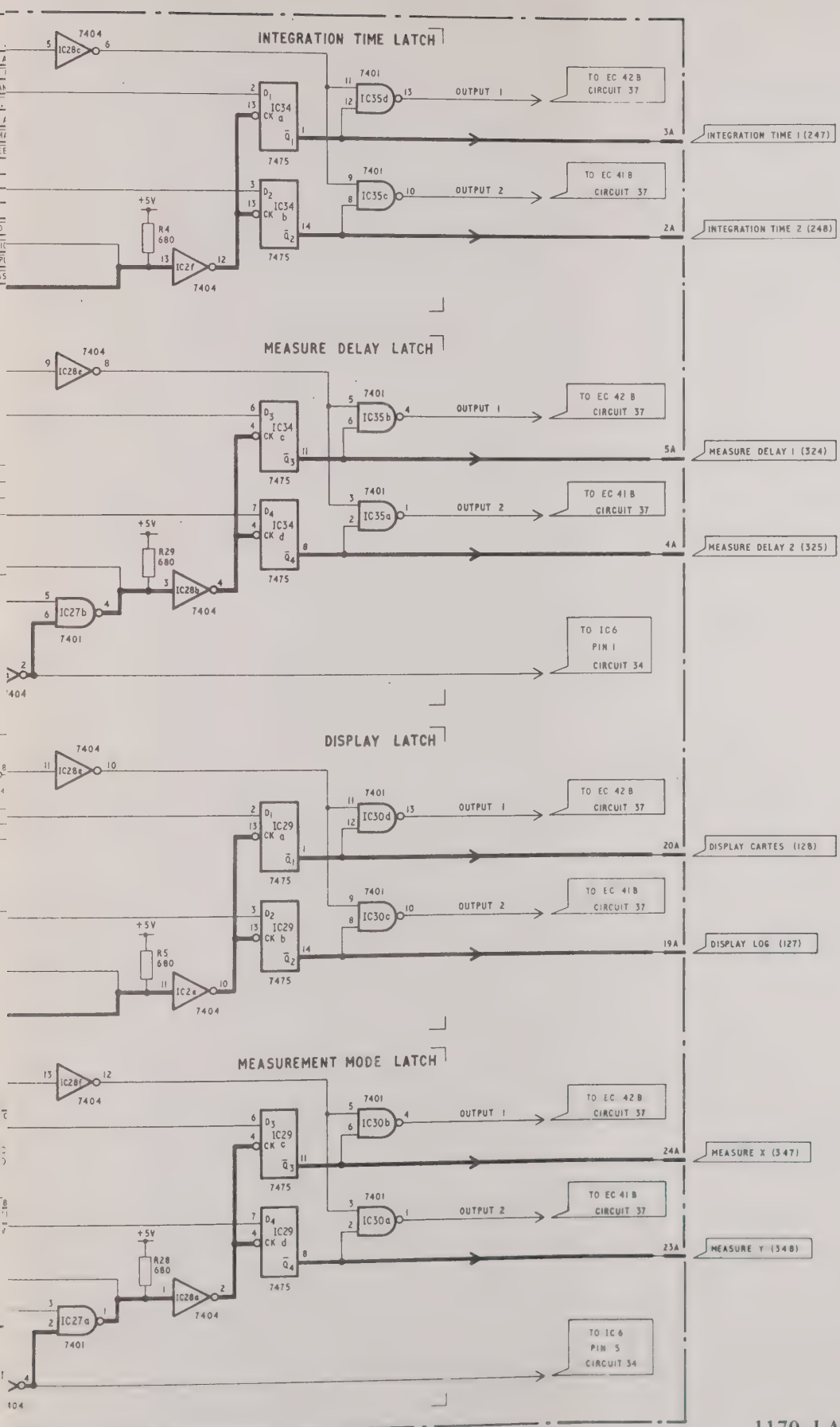
FROM IC26 PIN 8 CIRCUIT 31

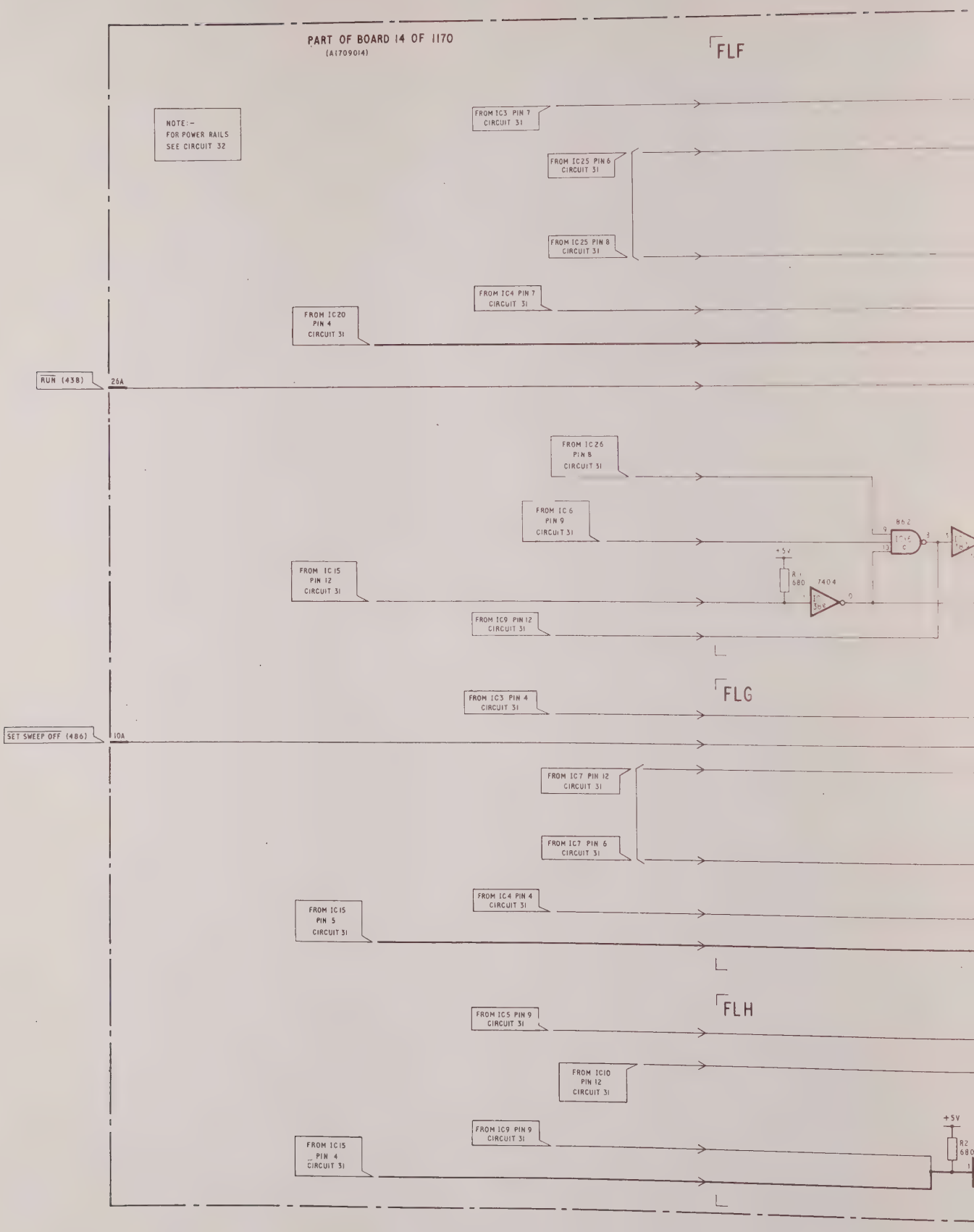
FROM IC15 PIN 10 CIRCUIT 31

+5V

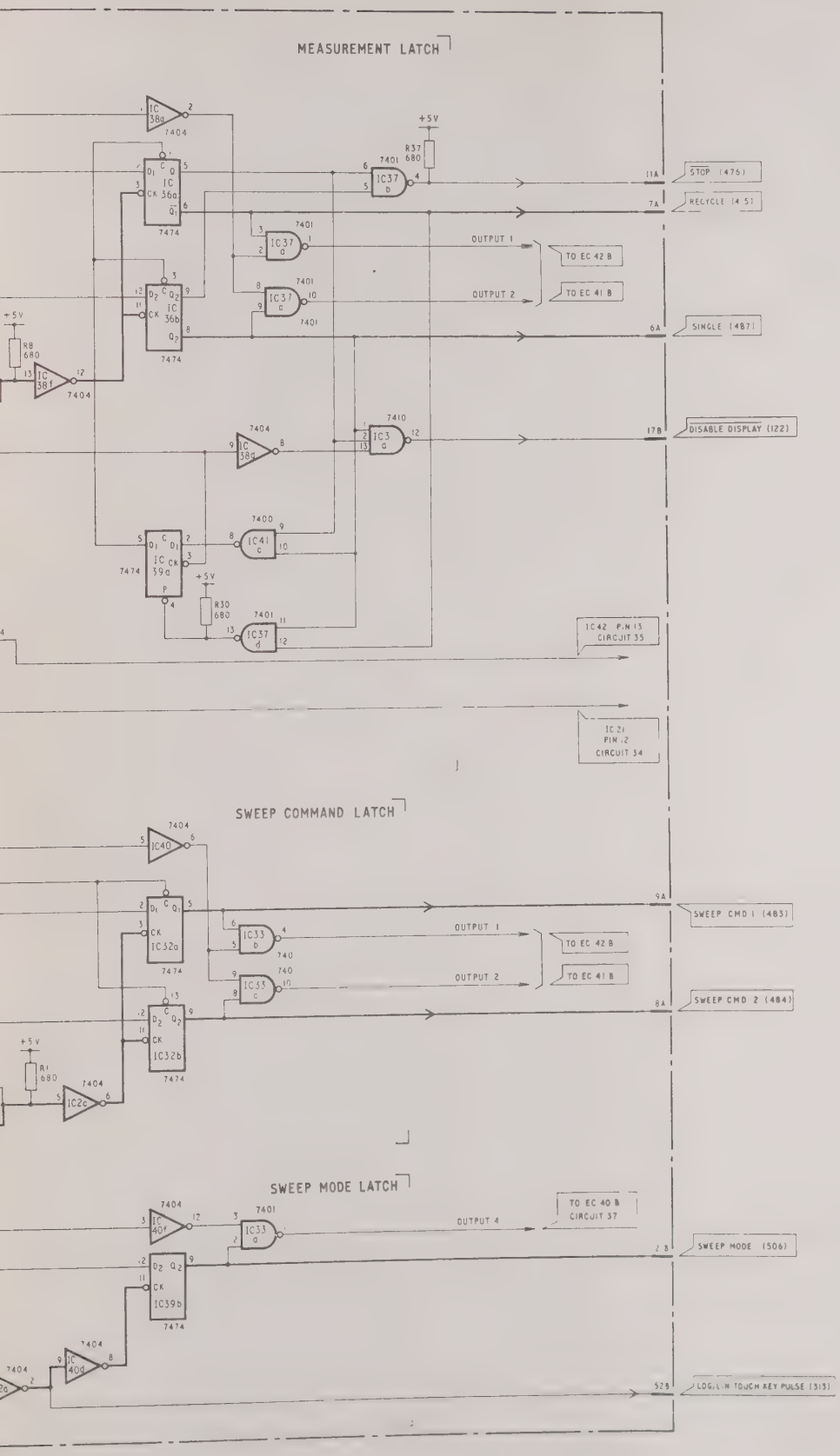
R25 680

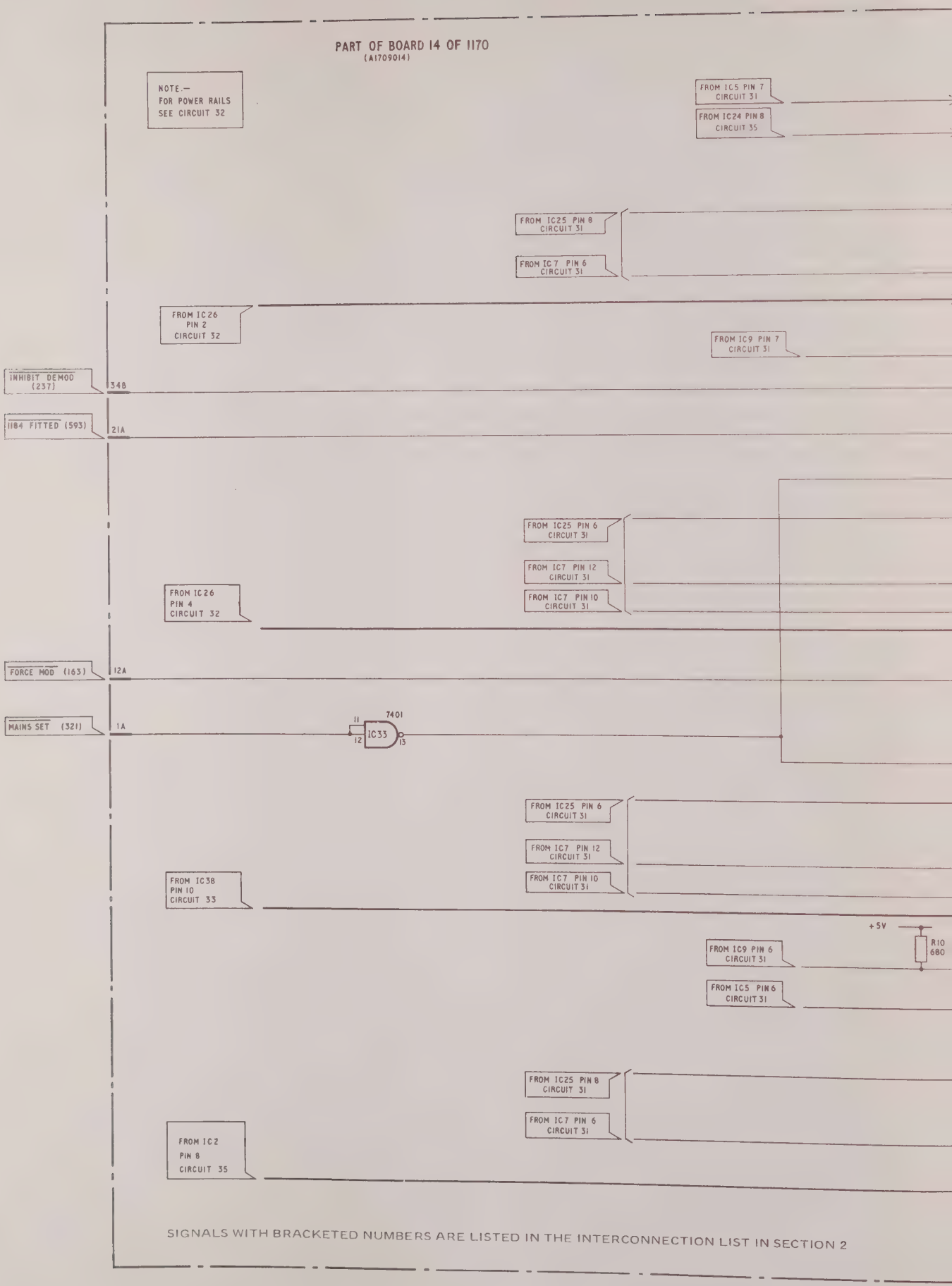
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

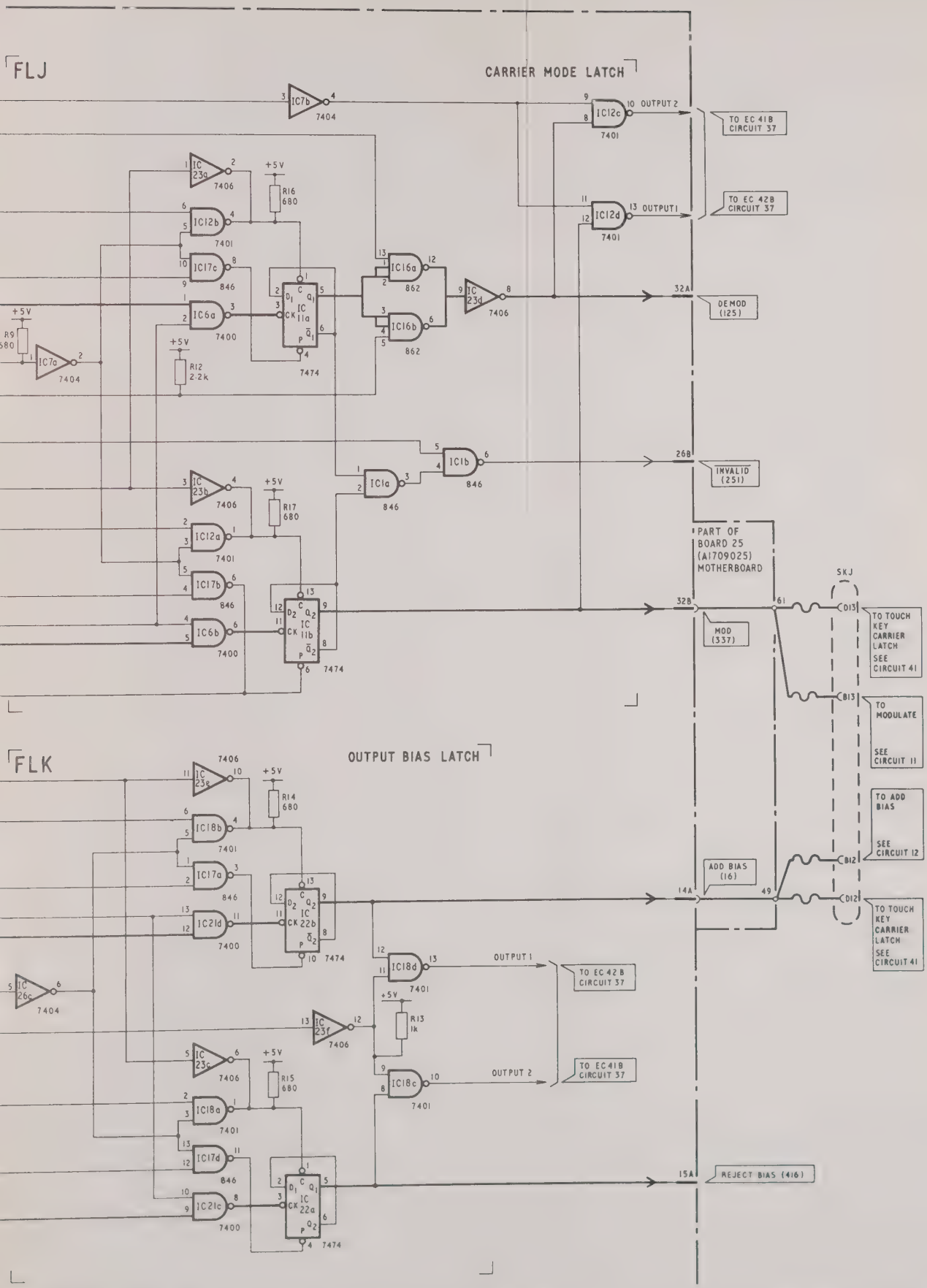

INTEGRATION TIME LATCH
MEASURE DELAY LATCH
DISPLAY LATCH
MEASUREMENT MODE LATCH
7404
7401
7475
+5V
R4 680
R29 680
R5 680
R28 680
OUTPUT 1
OUTPUT 2
TO EC 42B CIRCUIT 37
TO EC 41B CIRCUIT 37
TO IC6 PIN 1 CIRCUIT 34
TO IC6 PIN 5 CIRCUIT 34
3A
INTEGRATION TIME 1 (247)
2A
INTEGRATION TIME 2 (248)
5A
MEASURE DELAY 1 (324)
4A
MEASURE DELAY 2 (325)
20A
DISPLAY CARTES (128)
19A
DISPLAY LOG (127)
24A
MEASURE X (347)
23A
MEASURE Y (348)

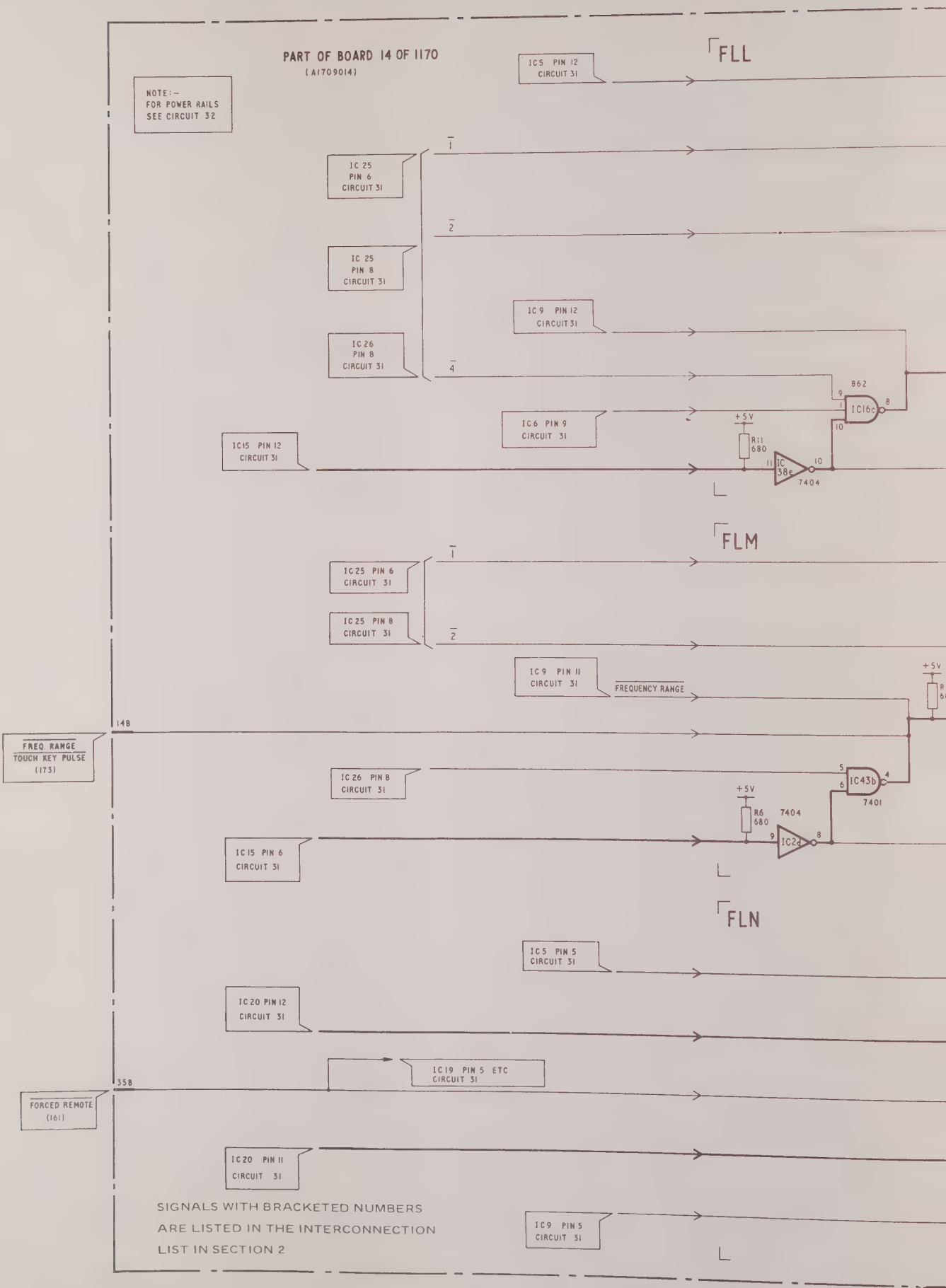


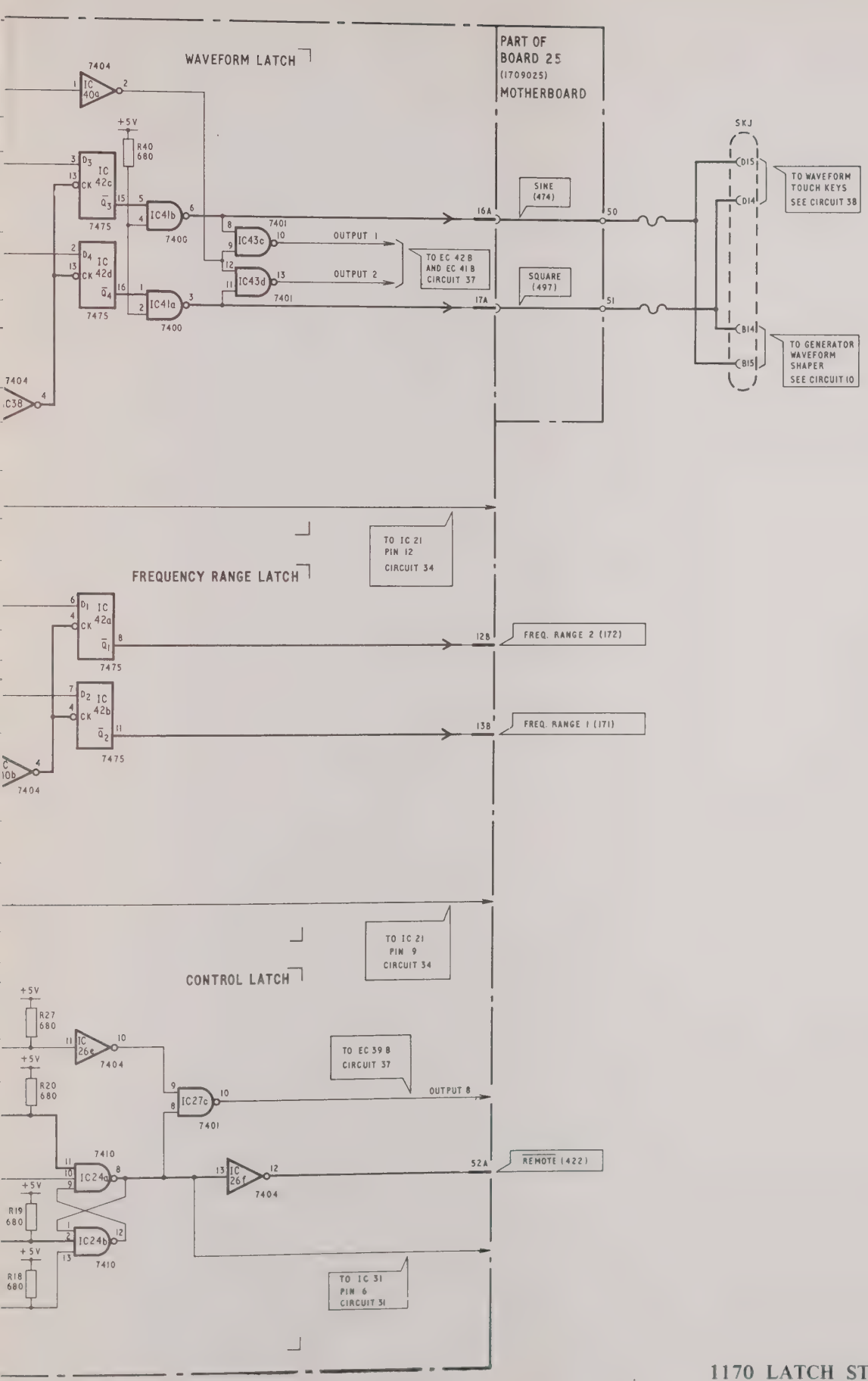
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

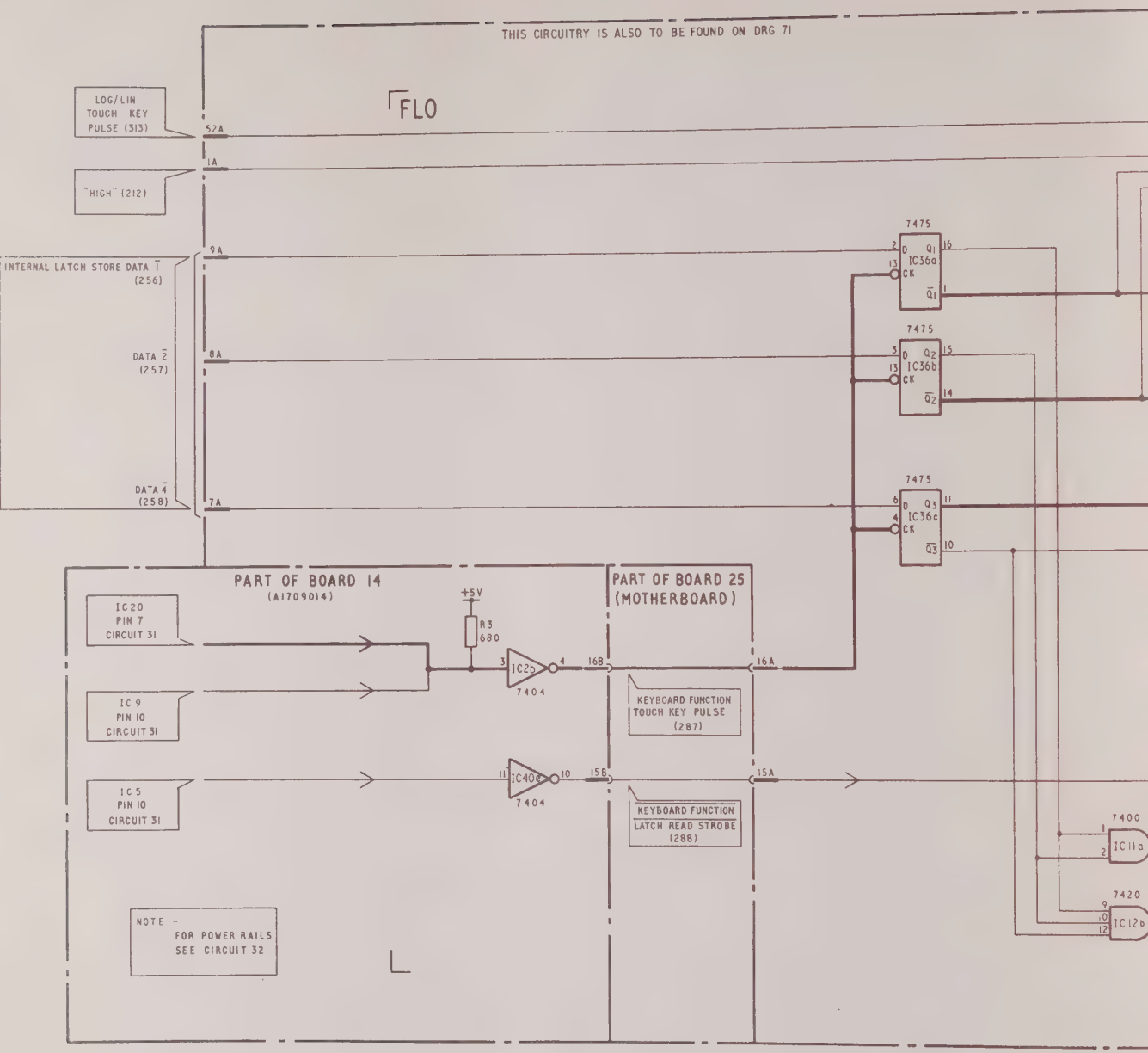

MEASUREMENT LATCH
IC 38a
7404
+5V
R37
680
7401
IC37 b
11A
STOP (476)
7A
RECYCLE (453)
IC 36a
7474
IC37 a
OUTPUT 1
TO EC 42 B
IC37 c
OUTPUT 2
TO EC 41 B
7401
IC 36b
7474
6A
SINGLE (487)
R8
680
IC 38f
7404
7404
IC 38g
7410
IC3 a
17B
DISABLE DISPLAY (122)
7400
IC41 c
IC 39a
7474
+5V
R30
680
7401
IC37 d
IC 42 P.N 13
CIRCUIT 35
IC 21
PIN 12
CIRCUIT 34
SWEEP COMMAND LATCH
7404
IC40
9A
SWEEP CMD 1 (483)
IC32a
7474
IC33 b
740
OUTPUT 1
TO EC 42 B
OUTPUT 2
IC33 c
740
TO EC 41 B
8A
SWEEP CMD 2 (484)
IC32b
7474
+5V
R1
680
7404
IC2c
SWEEP MODE LATCH
7404
IC 40f
7401
IC33 a
OUTPUT 4
TO EC 40 B
CIRCUIT 37
2 B
SWEEP MODE (506)
IC39b
7474
7404
IC 40d
7404
52B
LOGIC-N TOUCH KEY PULSE (313)


PART OF BOARD 14 OF 1170
(A1709014)
NOTE.—
FOR POWER RAILS
SEE CIRCUIT 32
FROM IC5 PIN 7
CIRCUIT 31
FROM IC24 PIN 8
CIRCUIT 35
FROM IC25 PIN 8
CIRCUIT 31
FROM IC7 PIN 6
CIRCUIT 31
FROM IC26
PIN 2
CIRCUIT 32
FROM IC9 PIN 7
CIRCUIT 31
INHIBIT DEMOD
(237)
34B
1184 FITTED (593)
21A
FROM IC25 PIN 6
CIRCUIT 31
FROM IC7 PIN 12
CIRCUIT 31
FROM IC7 PIN 10
CIRCUIT 31
FROM IC26
PIN 4
CIRCUIT 32
FORCE MOD (163)
12A
MAINS SET (321)
1A
7401
IC33
11
12
13
FROM IC25 PIN 6
CIRCUIT 31
FROM IC7 PIN 12
CIRCUIT 31
FROM IC7 PIN 10
CIRCUIT 31
FROM IC38
PIN 10
CIRCUIT 33
+5V
R10
680
FROM IC9 PIN 6
CIRCUIT 31
FROM IC5 PIN 6
CIRCUIT 31
FROM IC25 PIN 8
CIRCUIT 31
FROM IC7 PIN 6
CIRCUIT 31
FROM IC2
PIN 8
CIRCUIT 35
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

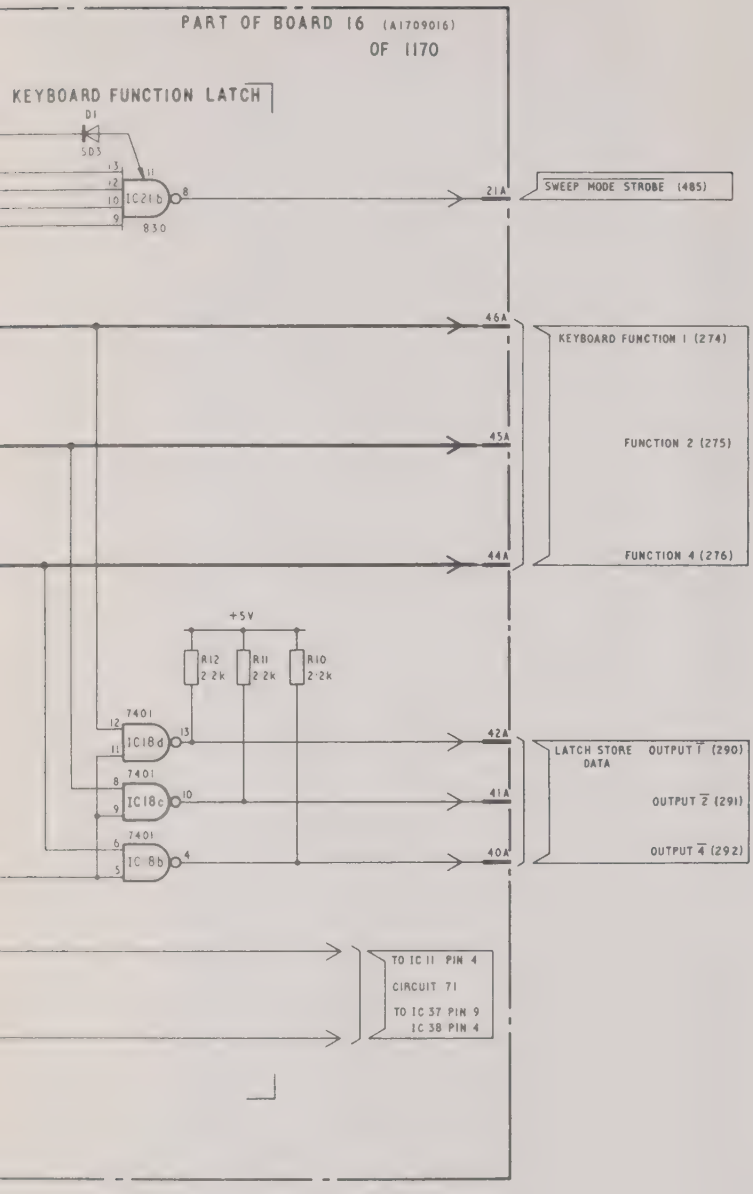

FLJ
CARRIER MODE LATCH
IC7b
7404
IC12c
7401
OUTPUT 2
TO EC 41B CIRCUIT 37
IC12d
7401
OUTPUT 1
TO EC 42B CIRCUIT 37
IC 23a
7406
+5V
R16 680
IC12b
7401
IC17c
846
IC 11a
7474
IC16a
862
IC16b
862
IC 23d
7406
32A
DEMOD (125)
+5V
R9 680
IC7a
7404
+5V
R12 2·2k
IC6a
7400
IC1b
846
26B
INVALID (251)
IC1a
846
IC 23b
7406
+5V
R17 680
IC12a
7401
IC17b
846
IC6b
7400
IC 11b
7474
PART OF BOARD 25 (A1709025) MOTHERBOARD
SKJ
32B
61
D13
TO TOUCH KEY CARRIER LATCH SEE CIRCUIT 41
MOD (337)
B13
TO MODULATE SEE CIRCUIT 11
TO ADD BIAS SEE CIRCUIT 12
ADD BIAS (16)
14A
49
B12
D12
TO TOUCH KEY CARRIER LATCH SEE CIRCUIT 41
FLK
OUTPUT BIAS LATCH
7406
IC 23e
+5V
R14 680
IC18b
7401
IC17a
846
IC 22b
7474
IC21d
7400
IC18d
7401
OUTPUT 1
TO EC 42B CIRCUIT 37
IC 26c
7404
IC 23f
7406
+5V
R13 1k
IC 23c
7406
+5V
R15 680
IC18c
7401
OUTPUT 2
TO EC 41B CIRCUIT 37
IC18a
7401
IC17d
846
IC 22a
7474
IC21c
7400
15A
REJECT BIAS (416)

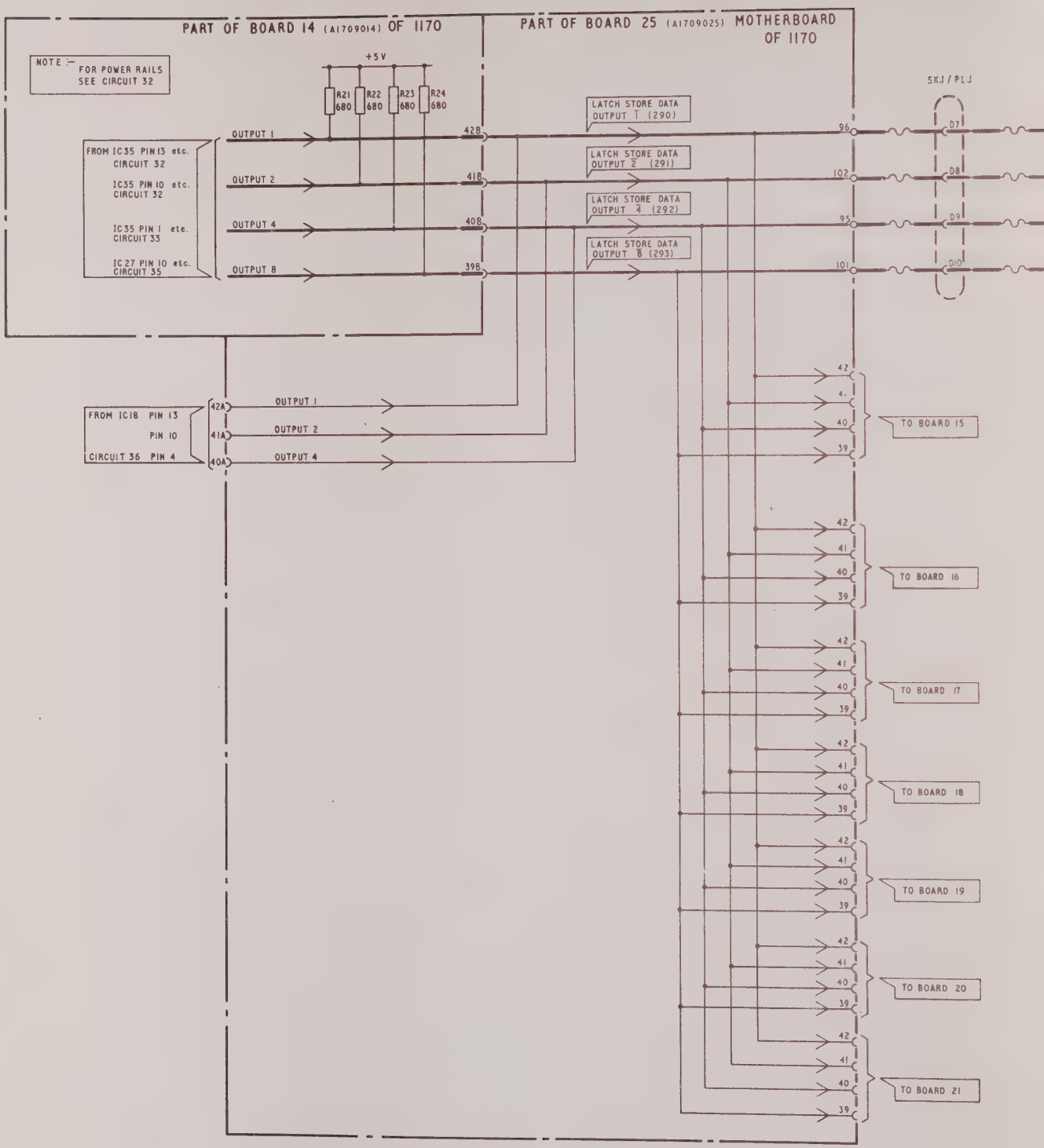

PART OF BOARD 14 OF 1170
(A1709014)
NOTE:-
FOR POWER RAILS
SEE CIRCUIT 32
IC5 PIN 12
CIRCUIT 31
FLL
IC 25
PIN 6
CIRCUIT 31
IC 25
PIN 8
CIRCUIT 31
IC 26
PIN 8
CIRCUIT 31
IC 9 PIN 12
CIRCUIT 31
IC 6 PIN 9
CIRCUIT 31
IC15 PIN 12
CIRCUIT 31
+5V
R11
680
IC
38c
7404
862
IC16c
FLM
IC25 PIN 6
CIRCUIT 31
IC25 PIN 8
CIRCUIT 31
IC 9 PIN 11
CIRCUIT 31
FREQUENCY RANGE
148
FREQ. RANGE
TOUCH KEY PULSE
(173)
IC 26 PIN 8
CIRCUIT 31
IC43b
7401
+5V
R6
680
7404
IC15 PIN 6
CIRCUIT 31
IC24
FLN
IC5 PIN 5
CIRCUIT 31
IC20 PIN 12
CIRCUIT 31
IC19 PIN 5 ETC
CIRCUIT 31
358
FORCED REMOTE
(161)
IC20 PIN 11
CIRCUIT 31
SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2
IC9 PIN 5
CIRCUIT 31


WAVEFORM LATCH
PART OF BOARD 25 (1709025) MOTHERBOARD
7404
IC 40a
+5V
R40 680
IC 42c
7475
IC41b
7400
IC 42d
IC41a
7401
IC43c
IC43d
OUTPUT 1
OUTPUT 2
TO EC 42B AND EC 41B CIRCUIT 37
SINE (474)
SQUARE (497)
16A
17A
50
51
SKJ
D15
D14
B14
B15
TO WAVEFORM TOUCH KEYS SEE CIRCUIT 38
TO GENERATOR WAVEFORM SHAPER SEE CIRCUIT 10
TO IC 21 PIN 12 CIRCUIT 34
FREQUENCY RANGE LATCH
IC 42a
IC 42b
12B
13B
FREQ. RANGE 2 (172)
FREQ. RANGE 1 (171)
TO IC 21 PIN 9 CIRCUIT 34
CONTROL LATCH
R27 680
R20 680
R19 680
R18 680
IC 26c
IC27c
IC24a
IC24b
IC 26f
7410
TO EC 39B CIRCUIT 37
OUTPUT 8
52A
REMOTE (422)
TO IC 31 PIN 6 CIRCUIT 31

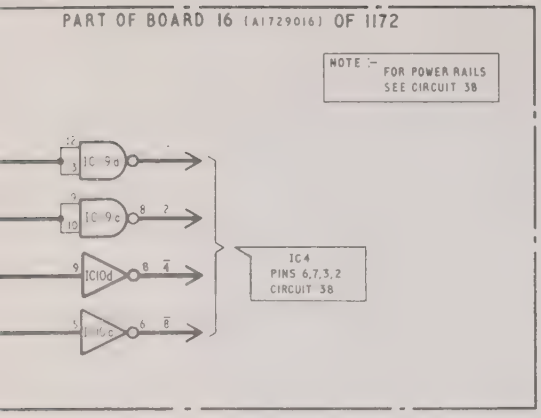


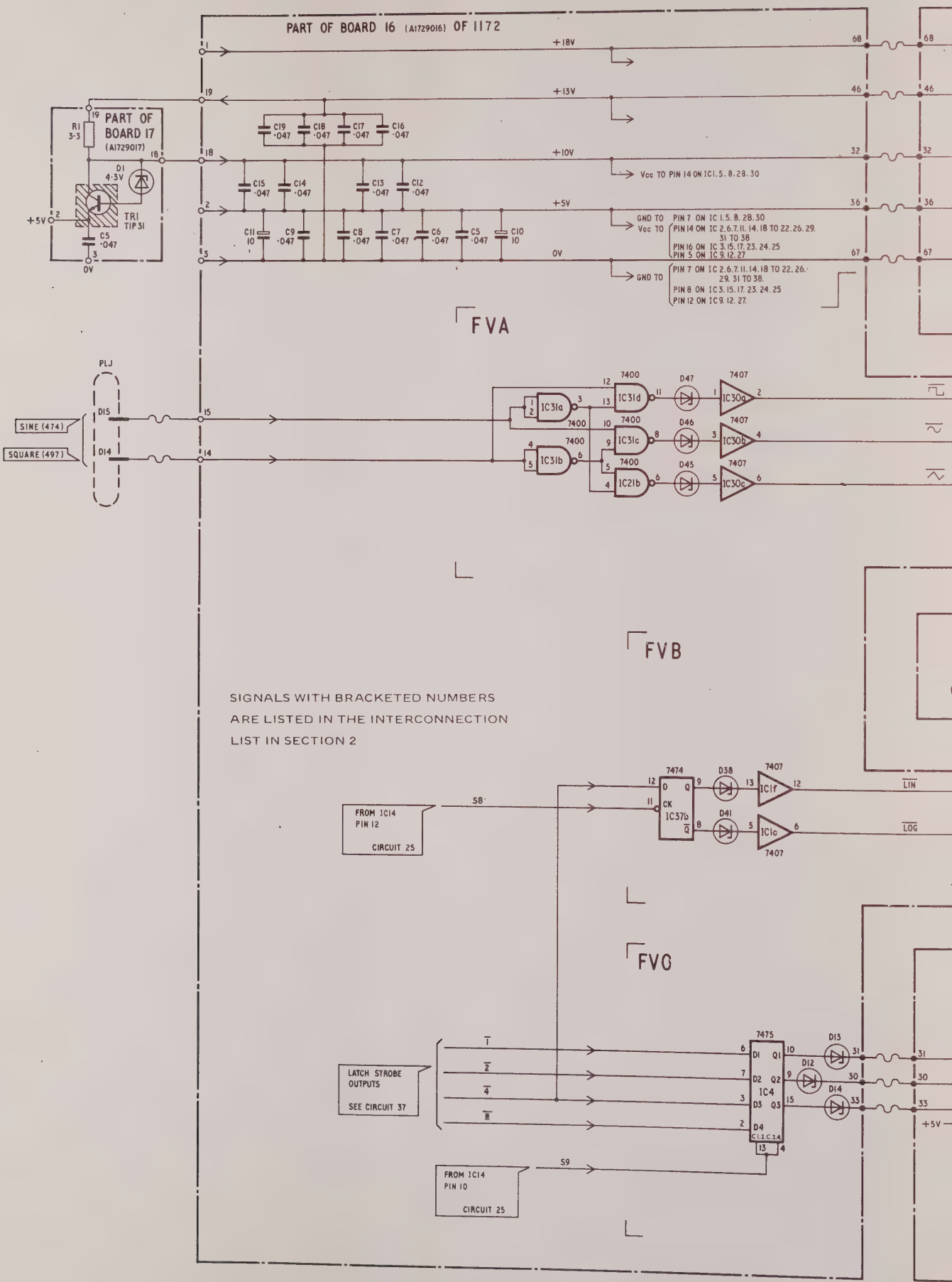
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

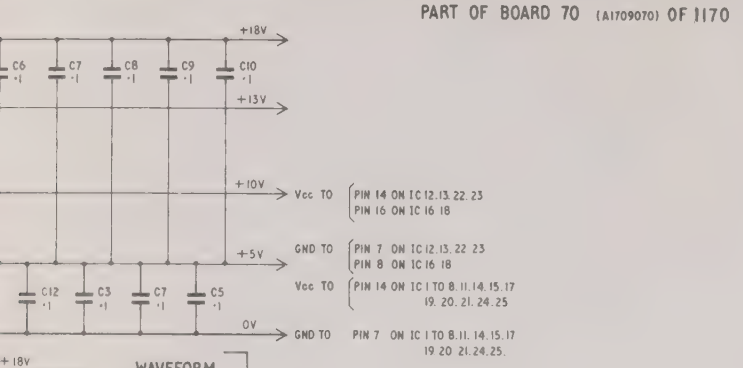

PART OF BOARD 16 (A1709016)
OF 1170
KEYBOARD FUNCTION LATCH
D1
SD3
IC21b
8
830
21A
SWEEP MODE STROBE (485)
46A
KEYBOARD FUNCTION 1 (274)
45A
FUNCTION 2 (275)
44A
FUNCTION 4 (276)
+5V
R12 2·2k
R11 2·2k
R10 2·2k
7401
IC18d
7401
IC18c
7401
IC 8b
42A
LATCH STORE DATA
OUTPUT 1 (290)
41A
OUTPUT 2 (291)
40A
OUTPUT 4 (292)
TO IC 11 PIN 4
CIRCUIT 71
TO IC 37 PIN 9
IC 38 PIN 4

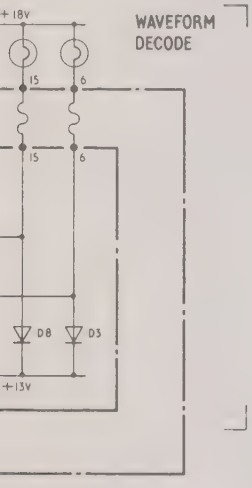


SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


PART OF BOARD 16 (A1729016) OF 1172
NOTE :- FOR POWER RAILS SEE CIRCUIT 38
IC 9a
IC 9c
IC10d
IC4 PINS 6,7,3,2 CIRCUIT 38

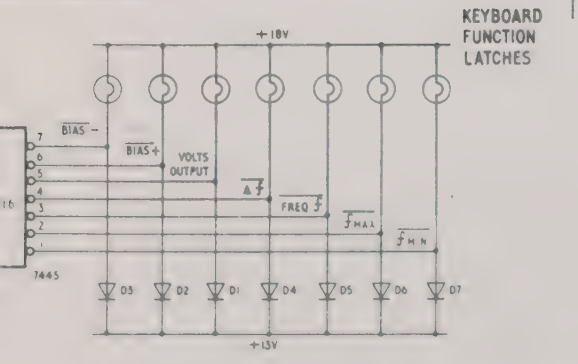

PART OF BOARD 16 (A1729016) OF 1172
+18V
+13V
+10V
+5V
0V
PART OF BOARD 17 (A1729017)
R1 3·3
D1 4·3V
TR1 TIP31
C5 ·047
C19 ·047
C18 ·047
C17 ·047
C16 ·047
C15 ·047
C14 ·047
C13 ·047
C12 ·047
C11 10
C9 ·047
C8 ·047
C7 ·047
C6 ·047
C5 ·047
C10 10
Vcc TO PIN 14 ON IC1. 5. 8. 28. 30
GND TO PIN 7 ON IC 1. 5. 8. 28. 30
Vcc TO PIN 14 ON IC 2. 6. 7. 11. 14. 18 TO 22. 26. 29. 31 TO 38.
PIN 16 ON IC 3. 15. 17. 23. 24. 25
PIN 5 ON IC 9. 12. 27.
GND TO PIN 7 ON IC 2. 6. 7. 11. 14. 18 TO 22. 26. 29. 31 TO 38.
PIN 8 ON IC 3. 15. 17. 23. 24. 25
PIN 12 ON IC 9. 12. 27.
FVA
PLJ
SINE (474)
SQUARE (497)
7400
IC31a
IC31b
IC31d
IC21b
7407
IC30a
IC30b
IC30c
D47
D46
D45
FVB
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2
FROM IC14 PIN 12 CIRCUIT 25
S8
7474
IC37b
IC1f
IC1e
D38
D41
LIN
LOG
FVC
LATCH STROBE OUTPUTS SEE CIRCUIT 37
7475
IC4
D13
D12
D14
S9
FROM IC14 PIN 10 CIRCUIT 25
+5V

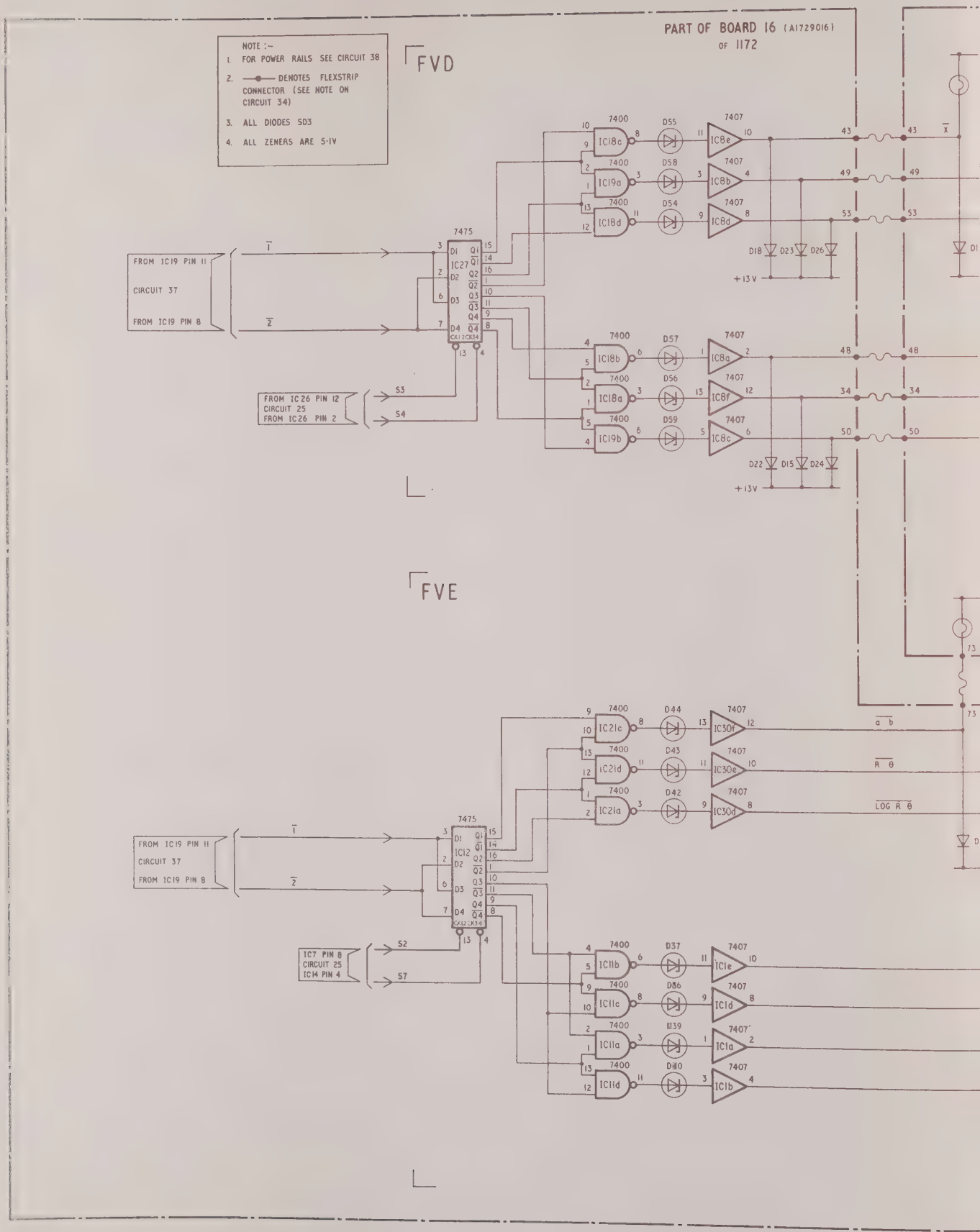


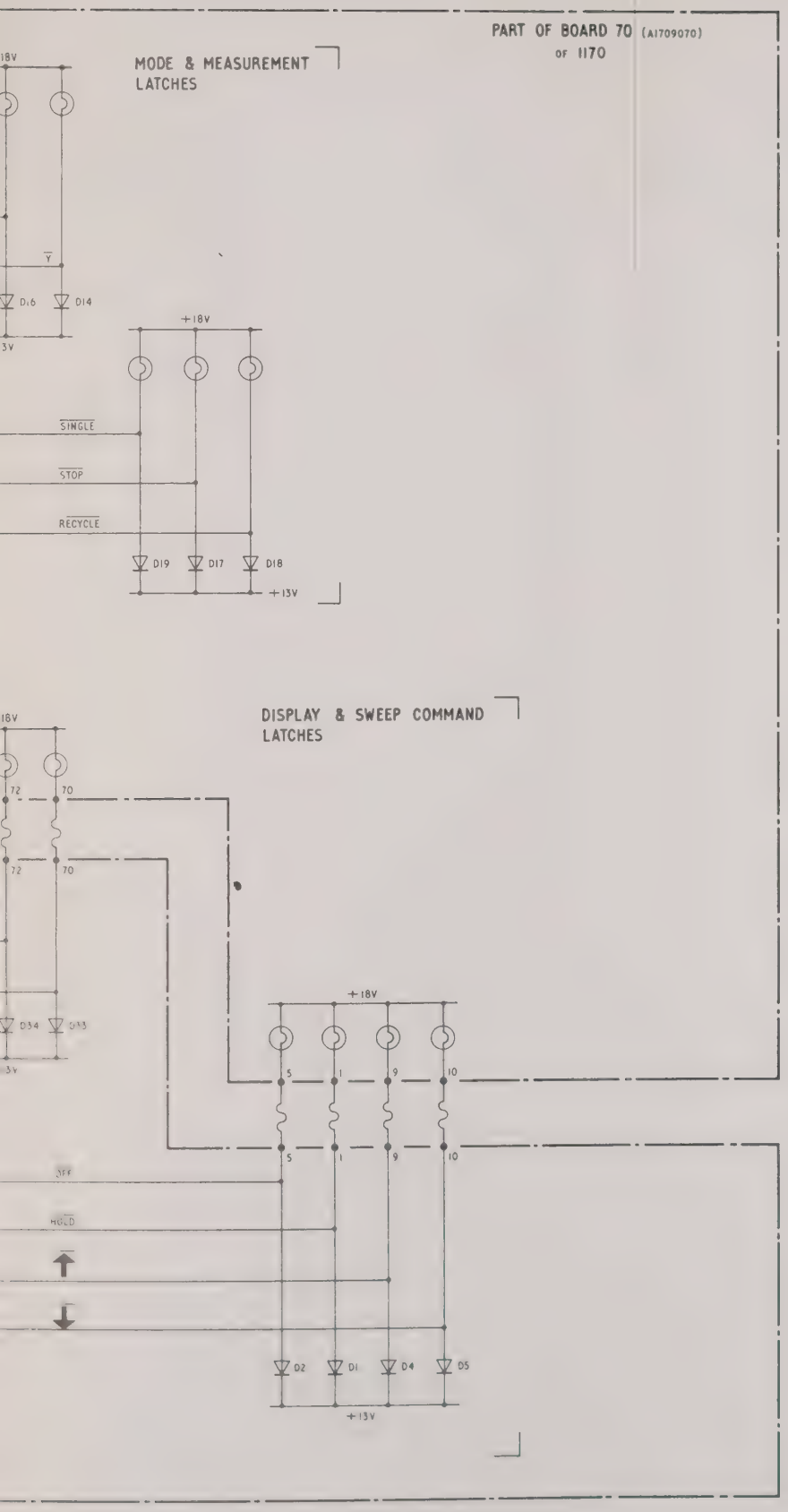


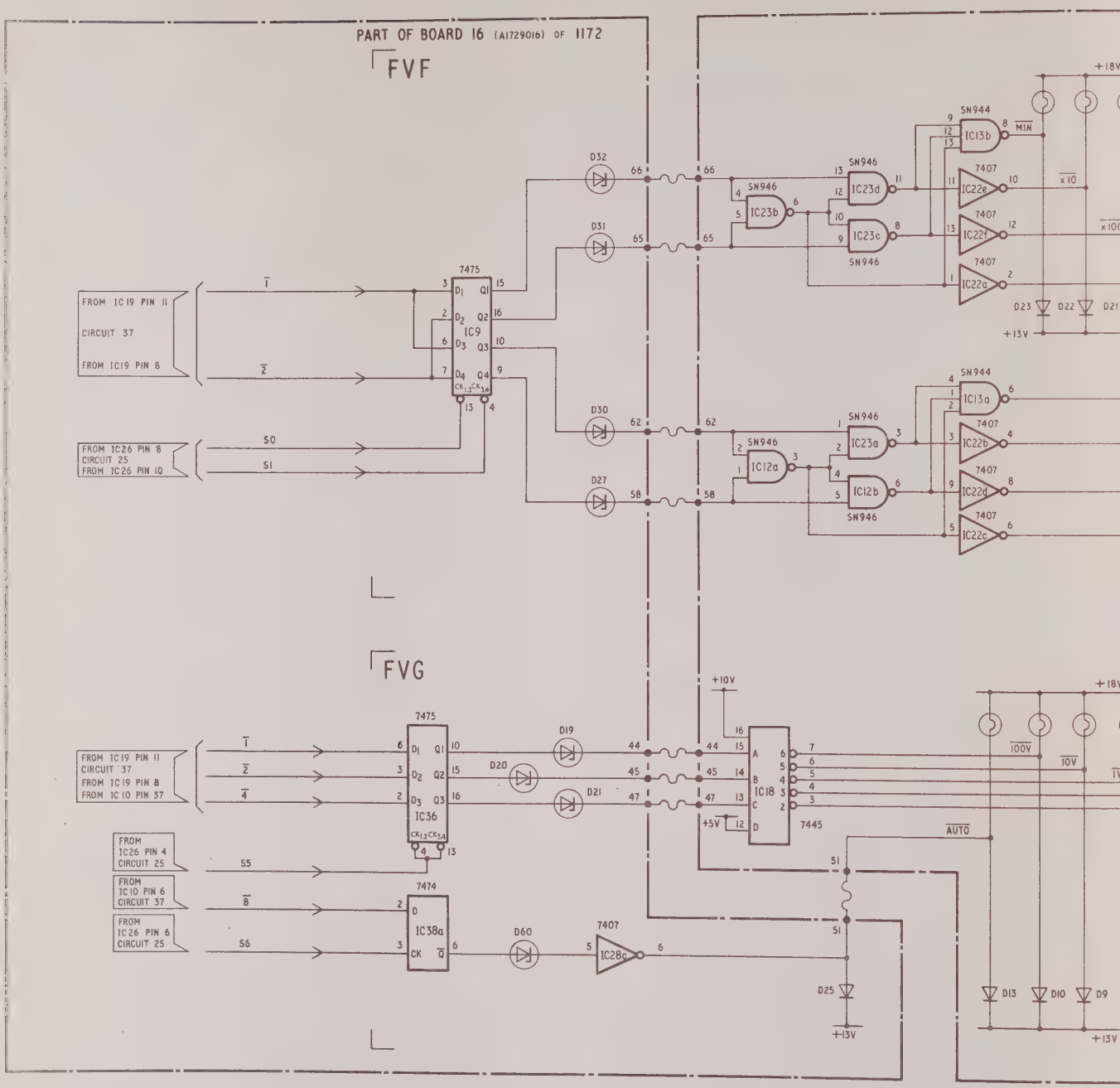
NOTE :-

1. BOARDS 16 & 70 ARE CONNECTED TOGETHER BY A LENGTH OF FLEXIBLE PRINTED CIRCUIT (FLEXSTRIP)
   —●— DENOTES FLEXSTRIP CONNECTOR
   —○— DENOTES TERMINAL PIN
2. ALL DIODES S03
3. ALL ZENERS. 5·1V UNLESS OTHERWISE STATED



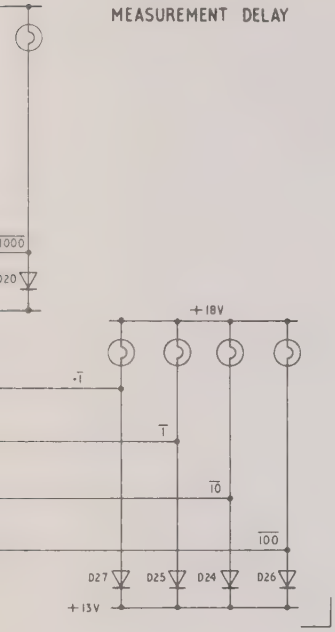

PART OF BOARD 16 (A1729016)
OF 1172
NOTE :-
1. FOR POWER RAILS SEE CIRCUIT 38
2. —●— DENOTES FLEXSTRIP CONNECTOR (SEE NOTE ON CIRCUIT 34)
3. ALL DIODES SD3
4. ALL ZENERS ARE 5·1V
FVD
FVE
7475
7400
7407
FROM IC19 PIN 11
CIRCUIT 37
FROM IC19 PIN 8
FROM IC26 PIN 12
CIRCUIT 25
FROM IC26 PIN 2
IC7 PIN 8
CIRCUIT 25
IC14 PIN 4
+13V


PART OF BOARD 70 (A1709070)
OF 1170
MODE & MEASUREMENT
LATCHES
+18V
Y
D16
D14
+18V
SINGLE
STOP
RECYCLE
D19
D17
D18
+13V
DISPLAY & SWEEP COMMAND
LATCHES
+18V
72
70
72
70
D34
D33
+18V
5
1
9
10
5
1
9
10
OFF
HOLD
D2
D1
D4
D5
+13V


PART OF BOARD 16 (A1729016) OF 1172
FVF
FVG
FROM IC19 PIN 11
CIRCUIT 37
FROM IC19 PIN 8
FROM IC26 PIN 8
CIRCUIT 25
FROM IC26 PIN 10
FROM IC19 PIN 11
CIRCUIT 37
FROM IC19 PIN 8
FROM IC10 PIN 37
FROM IC26 PIN 4
CIRCUIT 25
FROM IC10 PIN 6
CIRCUIT 37
FROM IC26 PIN 6
CIRCUIT 25
7475
IC9
IC36
7474
IC38a
7407
IC28c
SN946
IC23b
IC23d
IC23c
IC23a
IC12a
IC12b
SN944
IC13b
IC13a
7407
IC22e
IC22f
IC22a
IC22b
IC22d
IC22c
7445
IC18
D32
D31
D30
D27
D19
D20
D21
D60
D25
D23
D22
D21
D13
D10
D9
+18V
+13V
+10V
+5V
MIN
x10
x100
100V
10V
AUTO

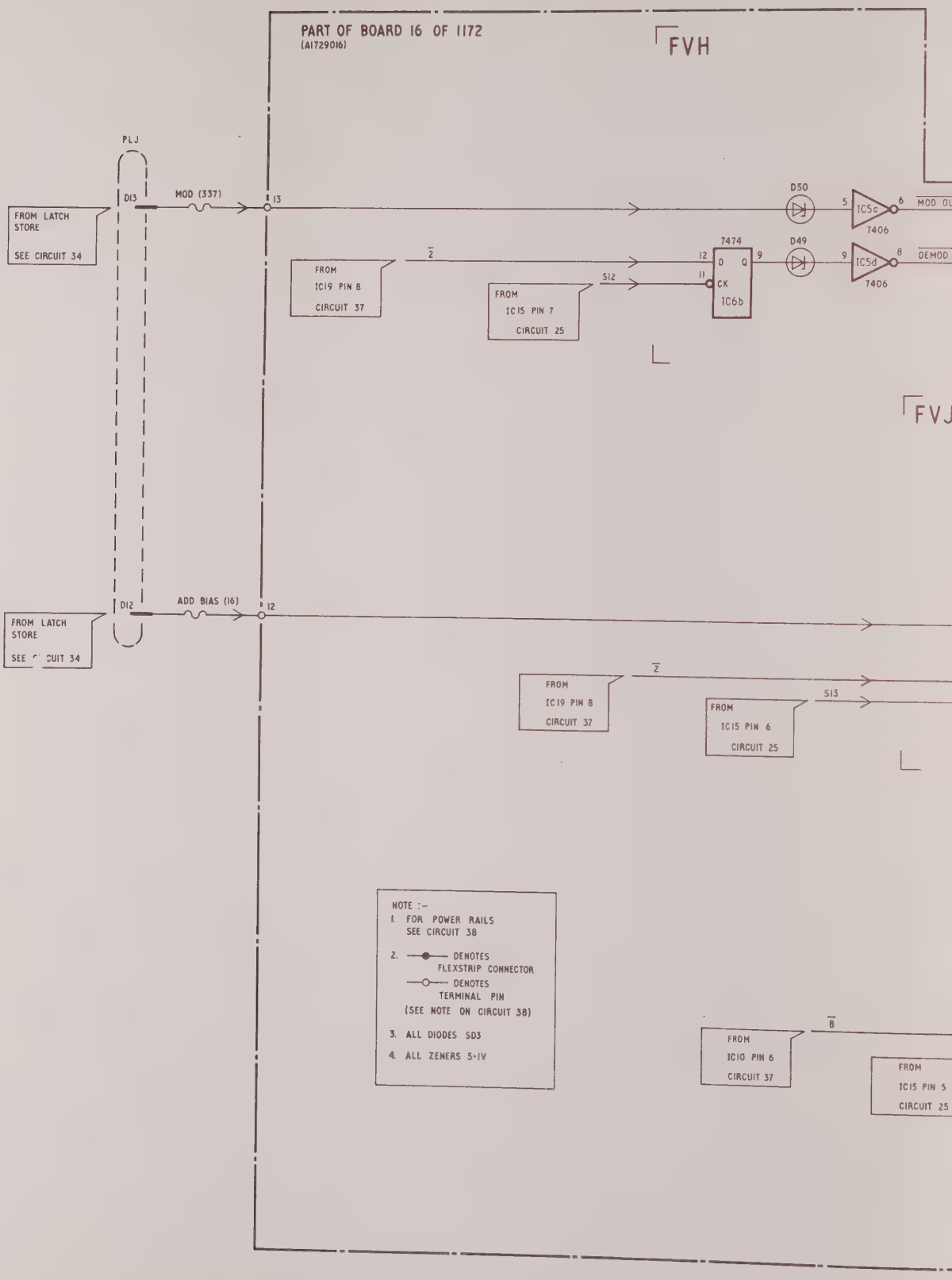
PART OF BOARD 70 (A1709070) OF 1170

INTEGRATION TIME &
MEASUREMENT DELAY

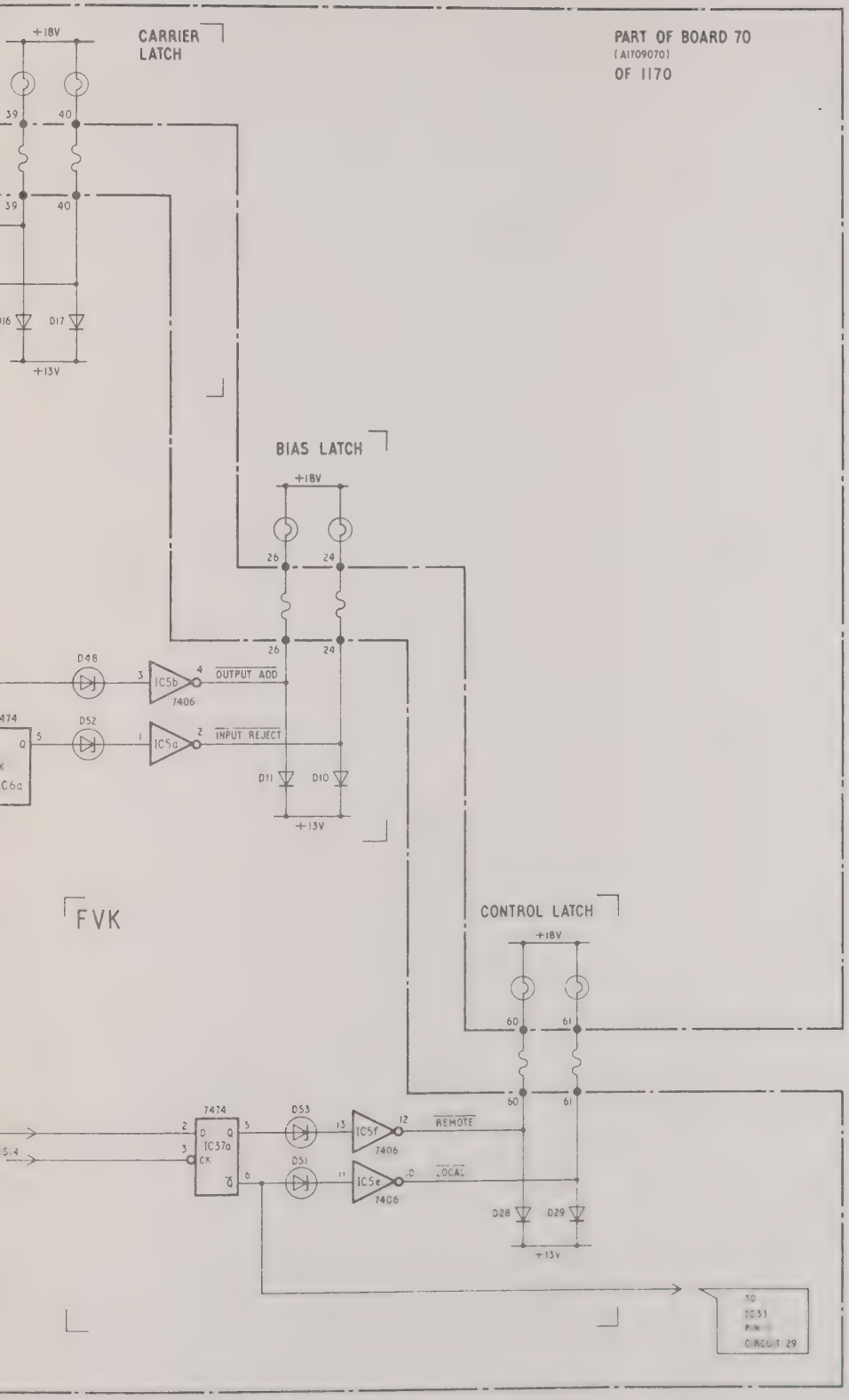


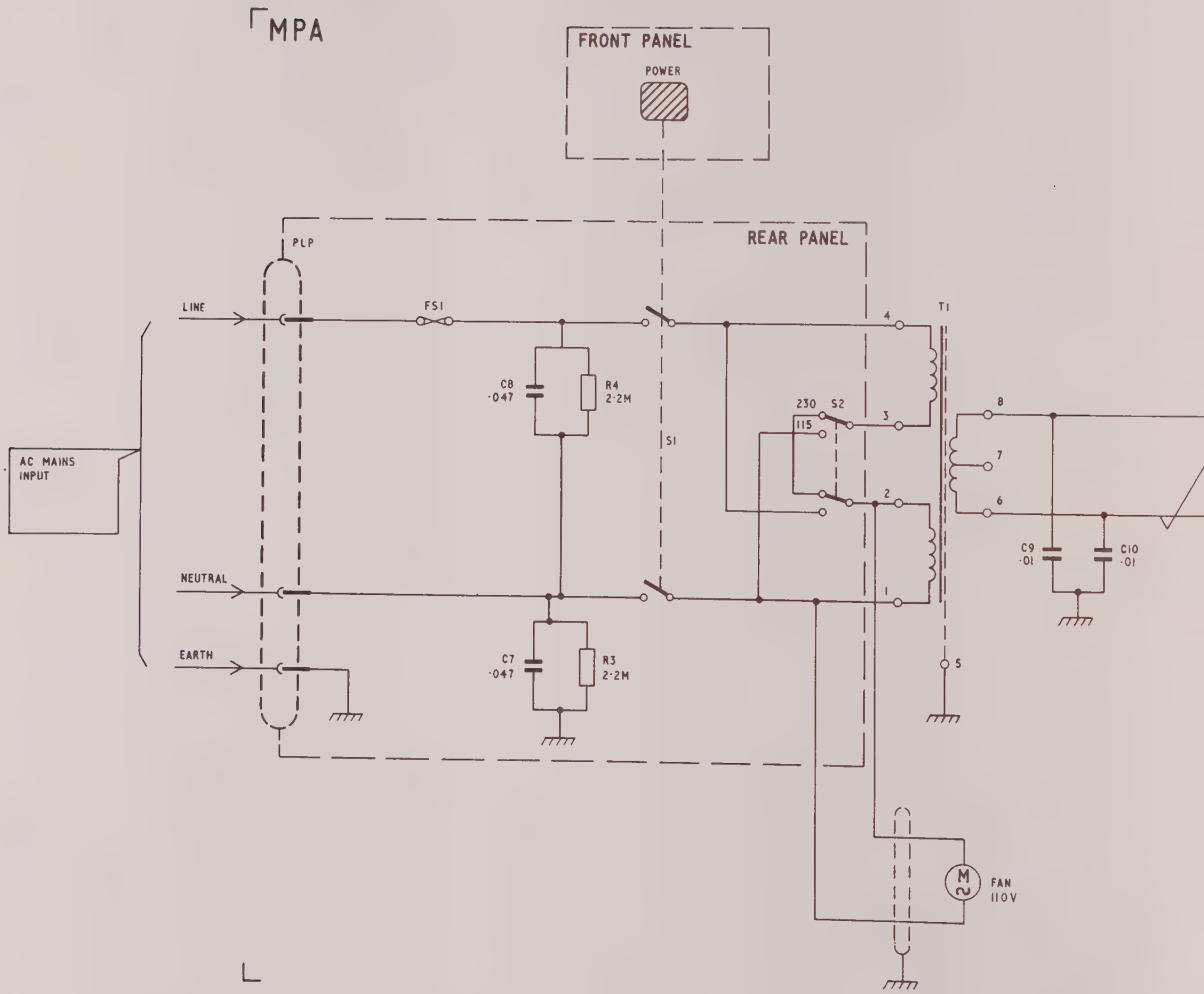
NOTE :-
1. FOR POWER RAILS SEE CIRCUIT 38
2. —●— DENOTES FLEX STRIP CONNECTOR
—○— DENOTES TERMINAL PIN
(SEE NOTE ON CIRCUIT 38)
3. ALL DIODES ARE SD3
4. ALL ZENERS ARE 5·1V

INPUT RANGE &
AUTO RANGE
LATCHES

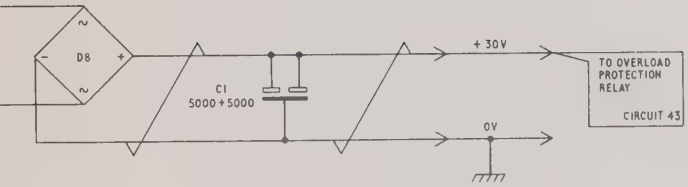


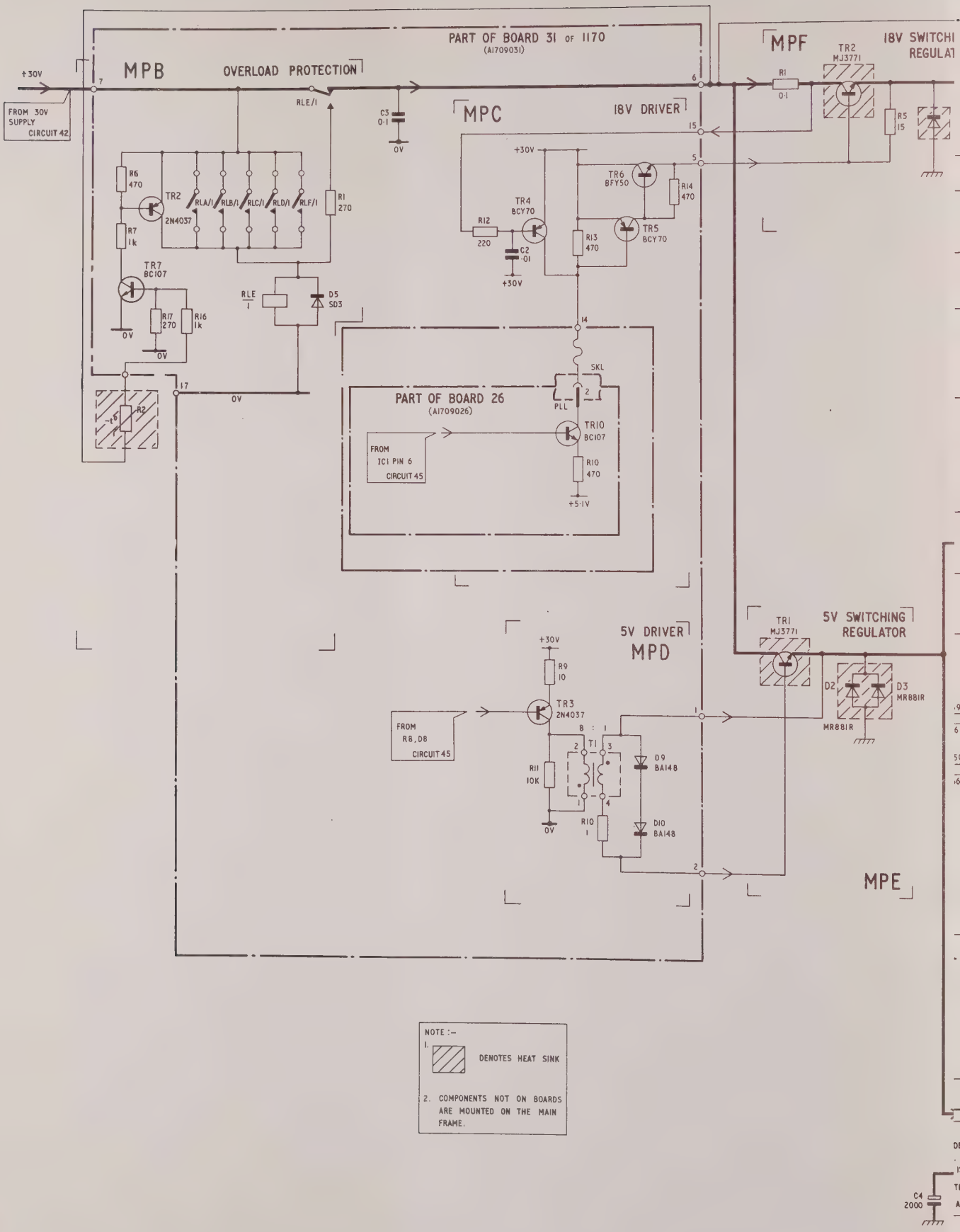
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


CARRIER LATCH
PART OF BOARD 70
[A1709070]
OF 1170
+18V
39
40
D16
D17
+13V
BIAS LATCH
26
24
D48
IC5b
7406
OUTPUT ADD
D52
IC5a
INPUT REJECT
D11
D10
FVK
CONTROL LATCH
60
61
7474
IC37a
D53
IC5f
REMOTE
D51
IC5e
LOCAL
D28
D29
TO
IC33
PIN
CIRCUIT 29


MPA
FRONT PANEL
POWER
REAR PANEL
PLP
LINE
FS1
C8
·047
R4
2·2M
S1
230
115
S2
T1
4
3
2
1
5
8
7
6
C9
·01
C10
·01
AC MAINS
INPUT
NEUTRAL
EARTH
C7
·047
R3
2·2M
M
2
FAN
110V

POWER INPUT &
30V SUPPLY
OF 1170

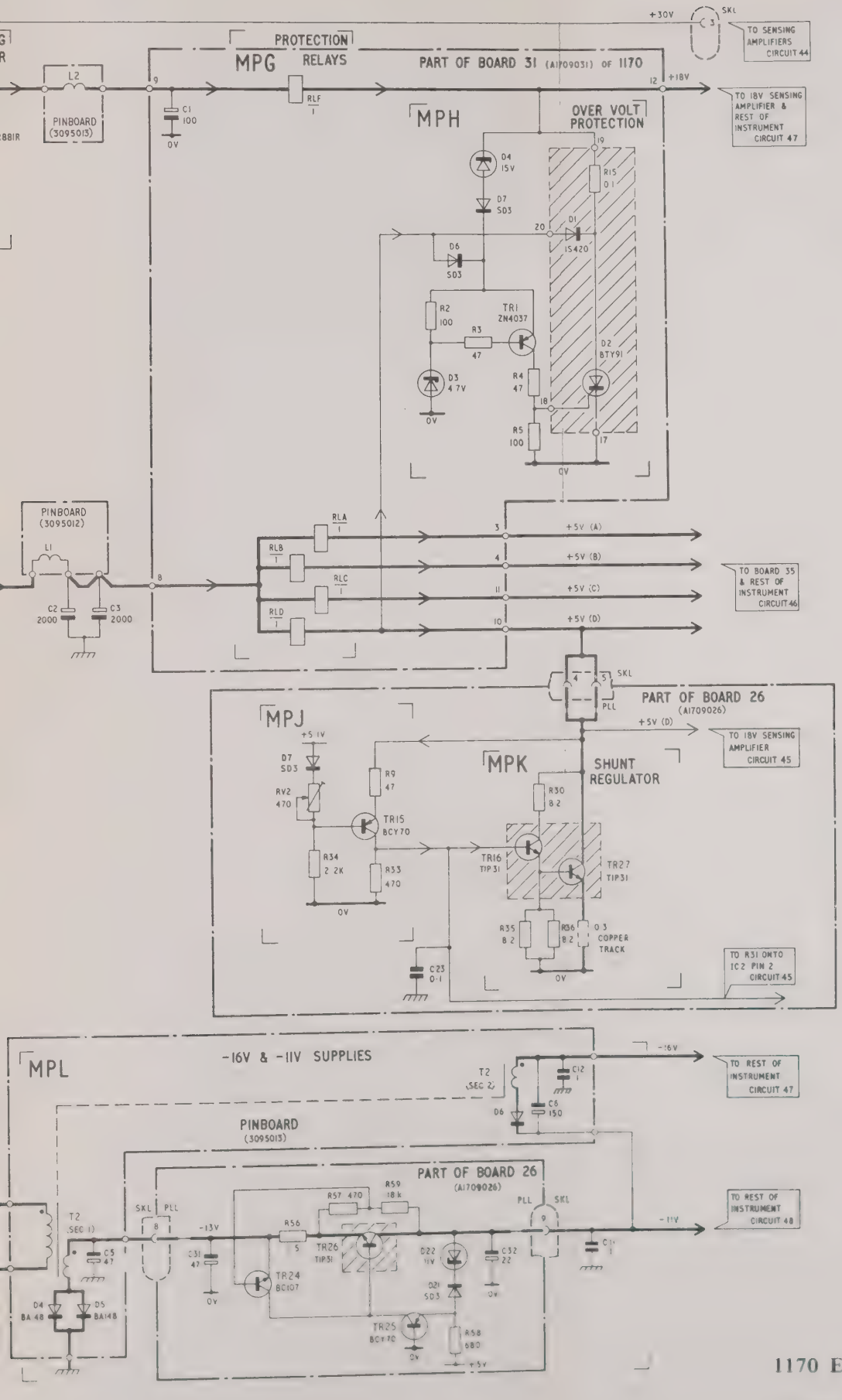


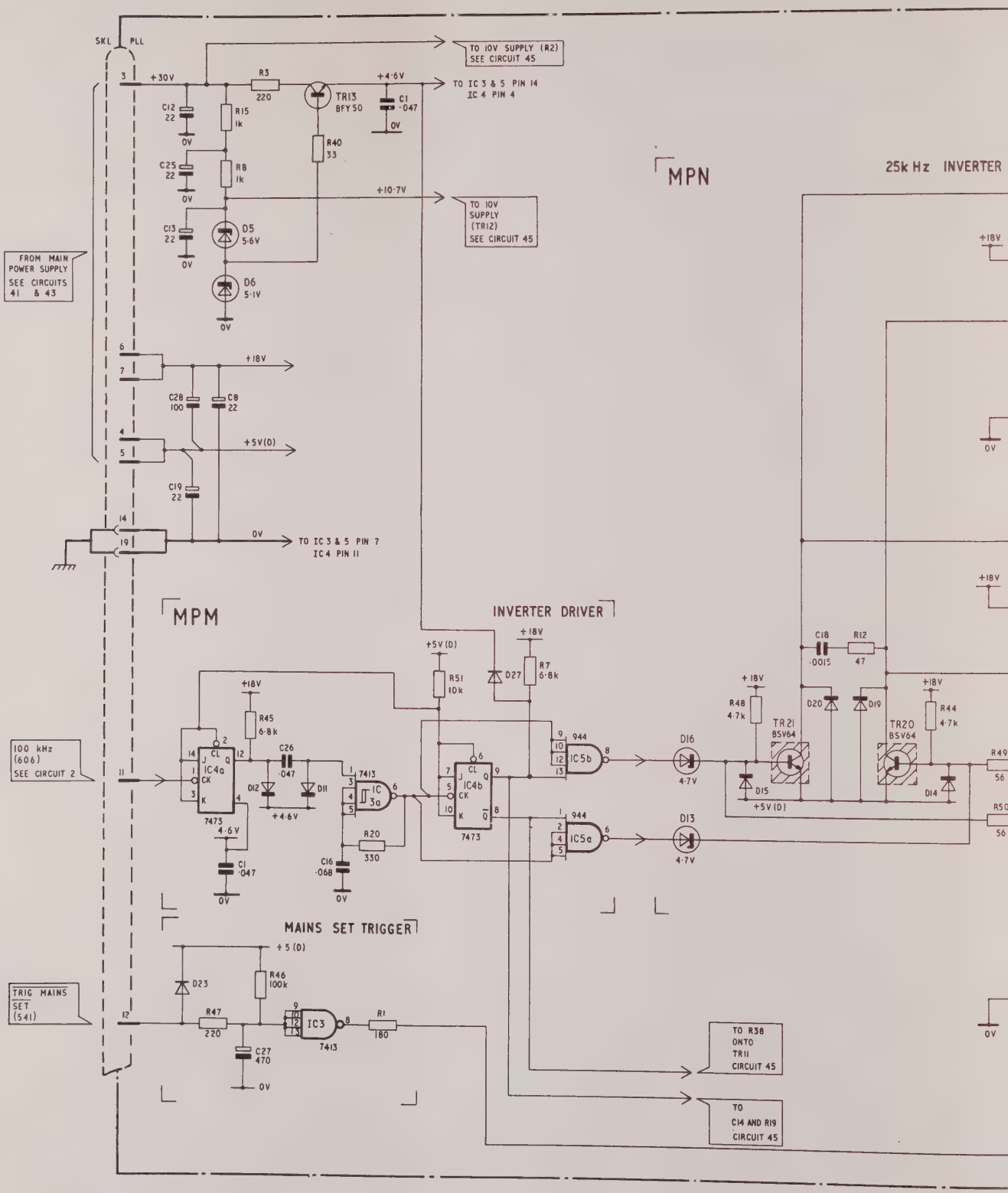


NOTE :–

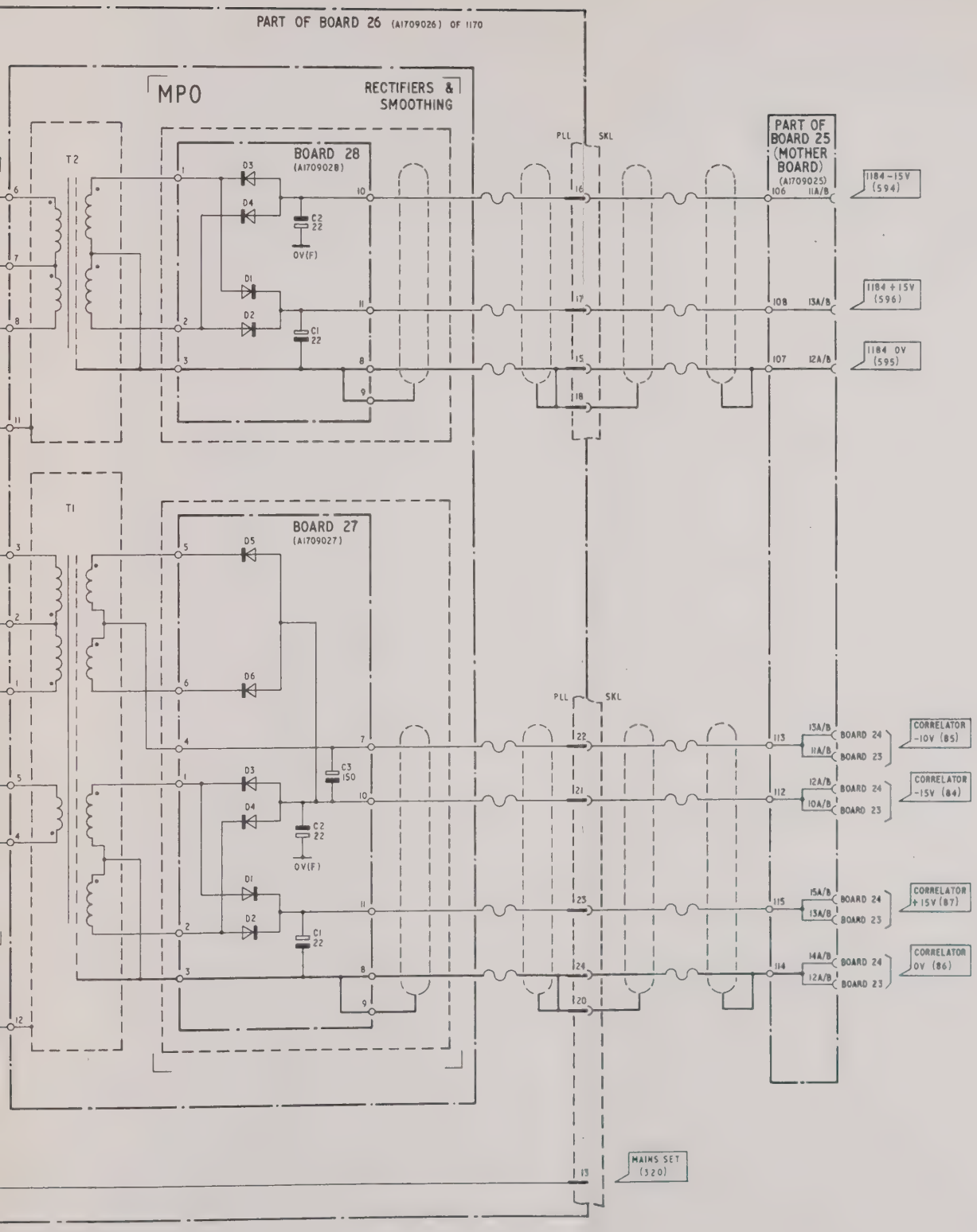
1. DENOTES HEAT SINK

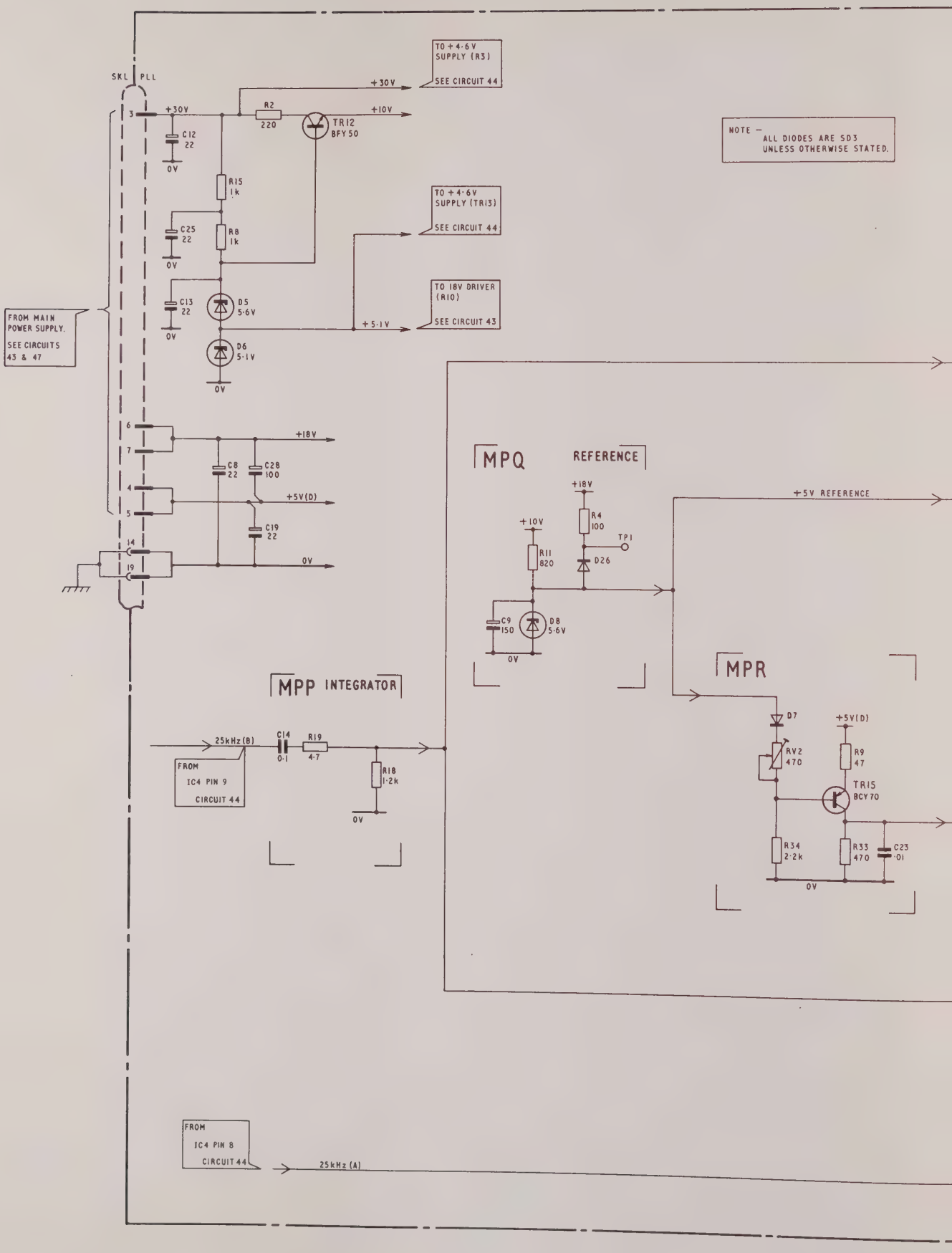
2. COMPONENTS NOT ON BOARDS ARE MOUNTED ON THE MAIN FRAME.

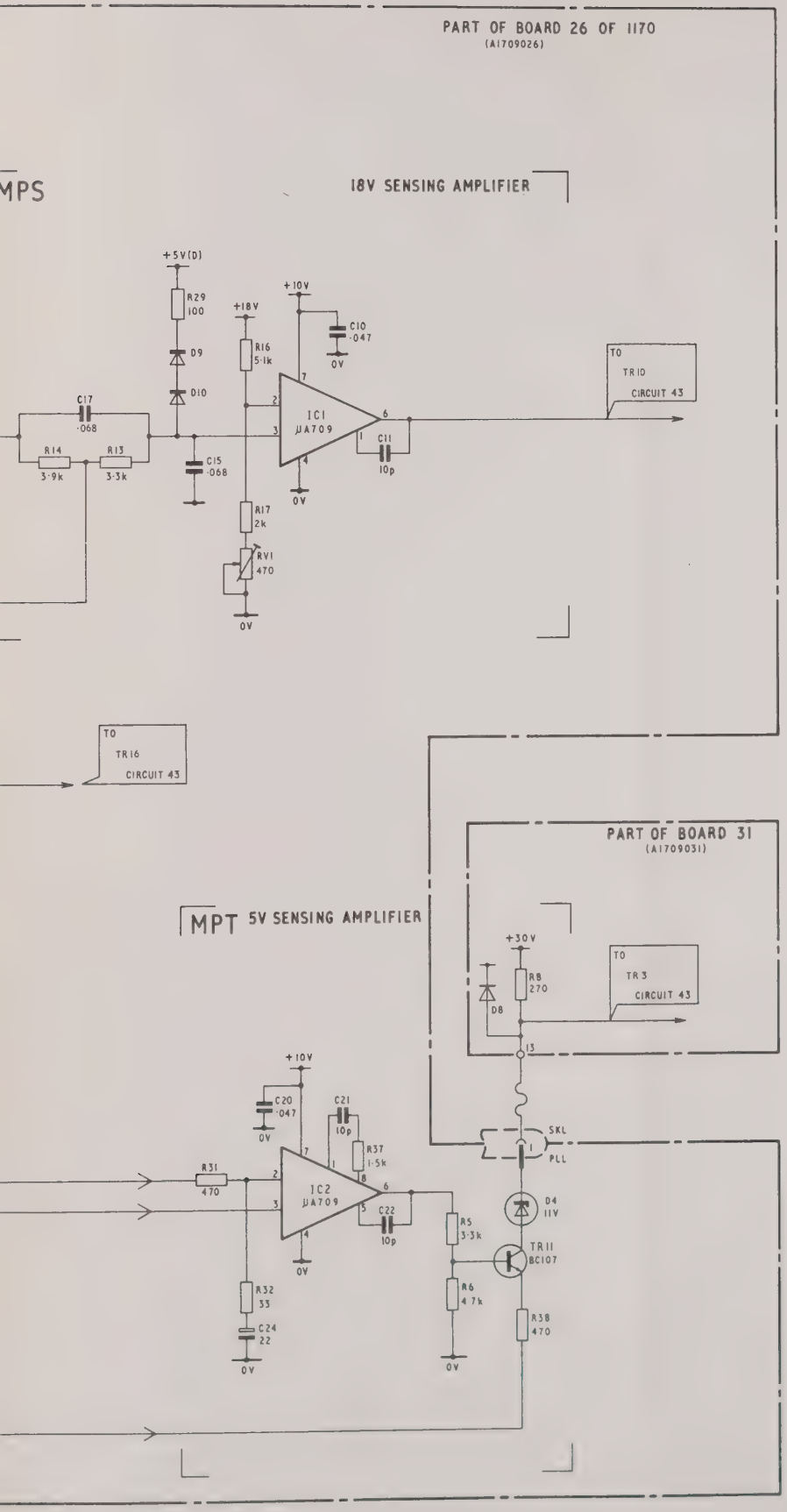

PROTECTION
MPG
RELAYS
PART OF BOARD 31 (AI709031) OF 1170
+30V
SKL
TO SENSING AMPLIFIERS CIRCUIT 44
+18V
TO 18V SENSING AMPLIFIER & REST OF INSTRUMENT CIRCUIT 47
L2
PINBOARD (3095013)
C1 100
0V
RLF
MPH
OVER VOLT PROTECTION
D4 15V
D7 S03
D6 S03
D1 IS420
R15 0·1
R2 100
R3 47
TR1 ZN4037
D3 4·7V
R4 47
D2 BTY91
R5 100
PINBOARD (3095012)
L1
C2 2000
C3 2000
RLA
RLB
RLC
RLD
+5V (A)
+5V (B)
+5V (C)
+5V (D)
TO BOARD 35 & REST OF INSTRUMENT CIRCUIT 46
MPJ
PART OF BOARD 26 (AI709026)
TO 18V SENSING AMPLIFIER CIRCUIT 45
MPK
SHUNT REGULATOR
D7 S03
RV2 470
R9 47
TR15 BCY70
R34 2·2K
R33 470
R30 8·2
TR16 TIP31
TR27 TIP31
R35 8·2
R36 8·2
0·3 COPPER TRACK
C23 0·1
TO R31 ONTO IC2 PIN 2 CIRCUIT 45
MPL
-16V & -11V SUPPLIES
T2 (SEC 2)
C12 1
D6
C6 150
-16V
TO REST OF INSTRUMENT CIRCUIT 47
PINBOARD (3095013)
PART OF BOARD 26 (AI709026)
T2 (SEC 1)
C5 47
D4 BA 48
D5 BA148
C31 47
-13V
R56 5
R57 470
R59 18k
TR24 BC107
TR26 TIP31
D22 11V
D21 S03
C32 22
TR25 BCY70
R58 680
+5V
-11V
TO REST OF INSTRUMENT CIRCUIT 48

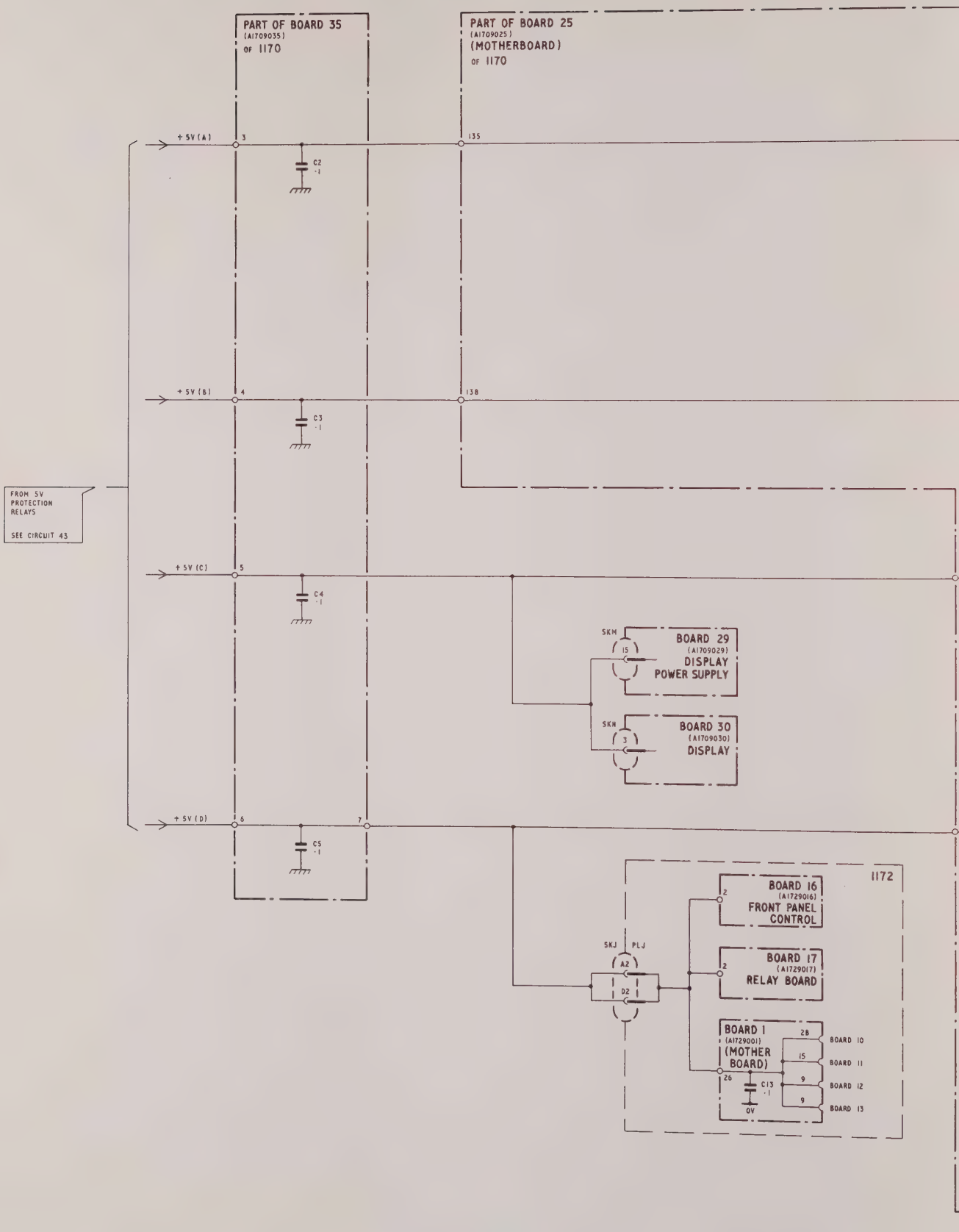


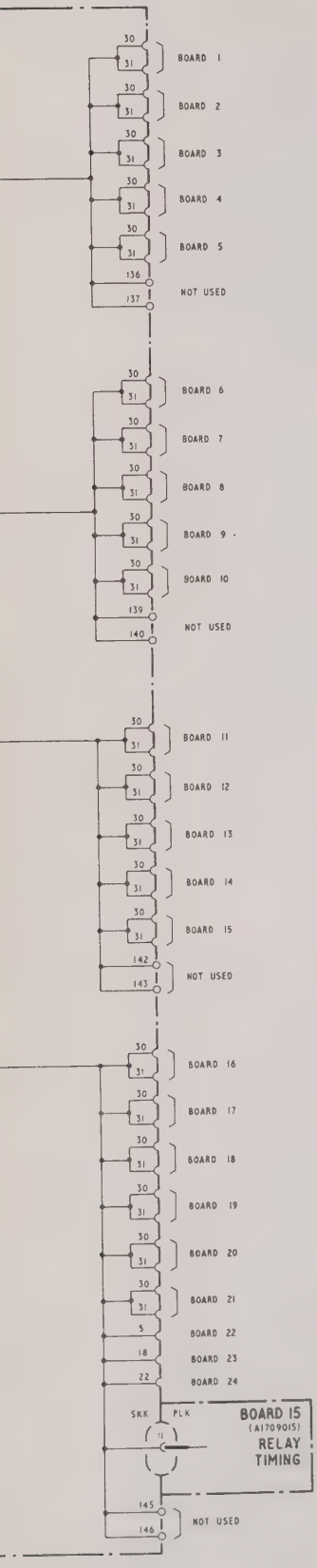
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

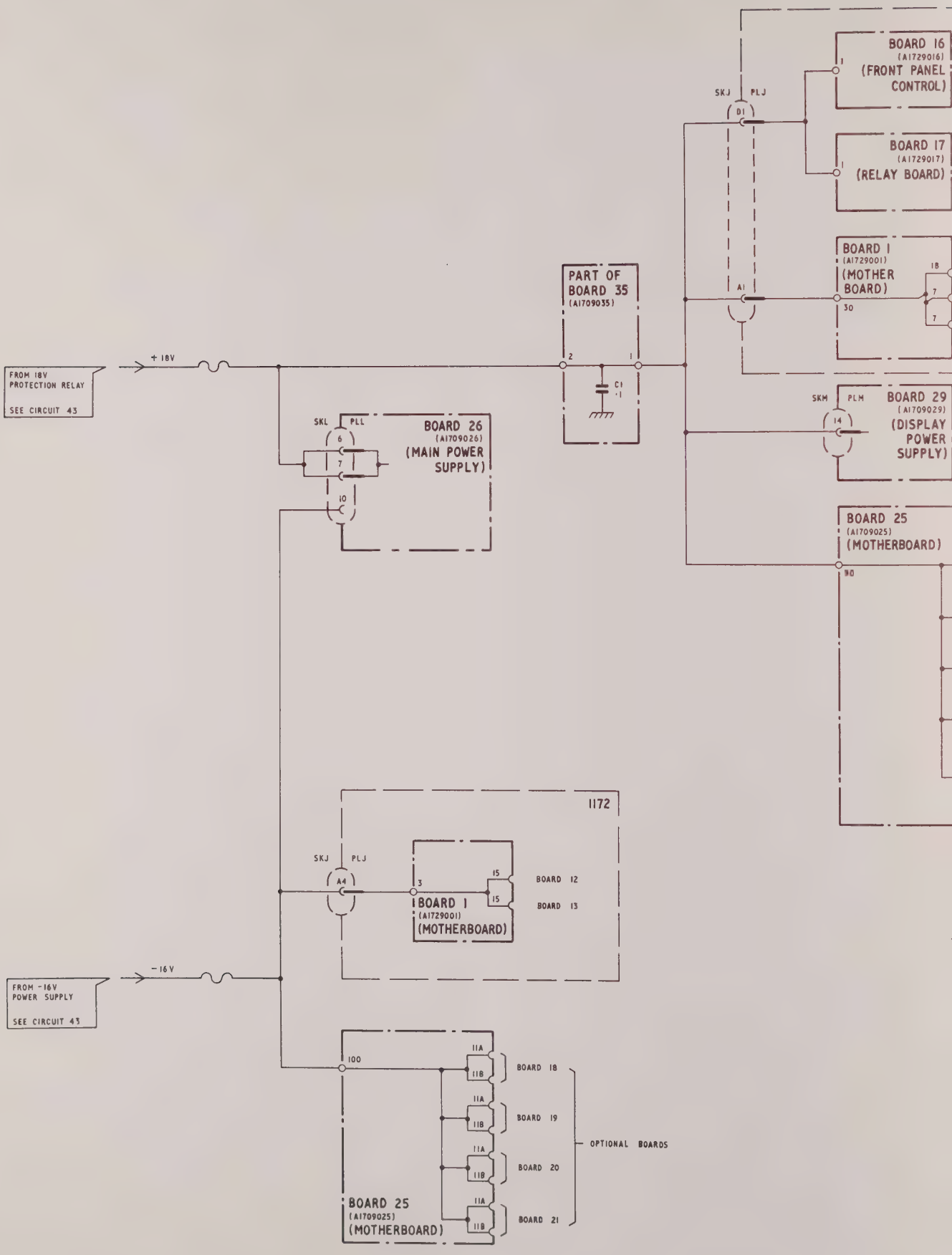

PART OF BOARD 26 (A1709026) OF 1170
MPO
RECTIFIERS & SMOOTHING
T2
T1
BOARD 28 (A1709028)
BOARD 27 (A1709027)
D1
D2
D3
D4
D5
D6
C1 22
C2 22
C3 150
0V(F)
PLL
SKL
PART OF BOARD 25 (MOTHER BOARD) (A1709025)
1184 -15V (594)
1184 +15V (596)
1184 0V (595)
CORRELATOR -10V (85)
CORRELATOR -15V (84)
CORRELATOR +15V (87)
CORRELATOR 0V (86)
BOARD 24
BOARD 23
MAINS SET (320)
ES A FLOATING SUPPLY
RE NO SUFFIX IS GIVEN
FERENCED TO EARTH
EAT SINK
D3 UNLESS OTHERWISE STATED


SKL PLL
+30V
TO +4·6V SUPPLY (R3)
SEE CIRCUIT 44
R2 220
TR12 BFY50
+10V
C12 22
0V
R15 1k
C25 22
R8 1k
TO +4·6V SUPPLY (TR13)
SEE CIRCUIT 44
C13 22
D5 5·6V
TO 18V DRIVER (R10)
SEE CIRCUIT 43
+5·1V
D6 5·1V
FROM MAIN POWER SUPPLY.
SEE CIRCUITS 43 & 47
NOTE – ALL DIODES ARE SD3 UNLESS OTHERWISE STATED.
+18V
C8 22
C28 100
+5V(D)
C19 22
MPQ REFERENCE
+18V
R4 100
+10V
R11 820
TP1
D26
+5V REFERENCE
C9 150
D8 5·6V
MPR
D7
+5V(D)
RV2 470
R9 47
TR15 BCY70
R34 2·2k
R33 470
C23 ·01
MPP INTEGRATOR
25kHz(B)
C14 0·1
R19 4·7
FROM IC4 PIN 9 CIRCUIT 44
R18 1·2k
FROM IC4 PIN 8 CIRCUIT 44
25kHz (A)

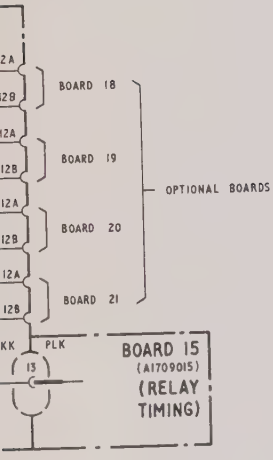

PART OF BOARD 26 OF 1170
(A1709026)
MPS
18V SENSING AMPLIFIER
+5V(D)
R29
100
D9
D10
+18V
R16
5·1k
+10V
C10
·047
0V
TO
TR10
CIRCUIT 43
C17
·068
R14
3·9k
R13
3·3k
C15
·068
IC1
µA709
C11
10p
R17
2k
RV1
470
0V
TO
TR16
CIRCUIT 43
PART OF BOARD 31
(A1709031)
MPT 5V SENSING AMPLIFIER
+30V
R8
270
D8
TO
TR3
CIRCUIT 43
13
SKL
PLL
+10V
C20
·047
C21
10p
R37
1·5k
R31
470
IC2
µA709
C22
10p
D4
11V
R5
3·3k
TR11
BC107
R6
4·7k
R38
470
R32
33
C24
22
0V

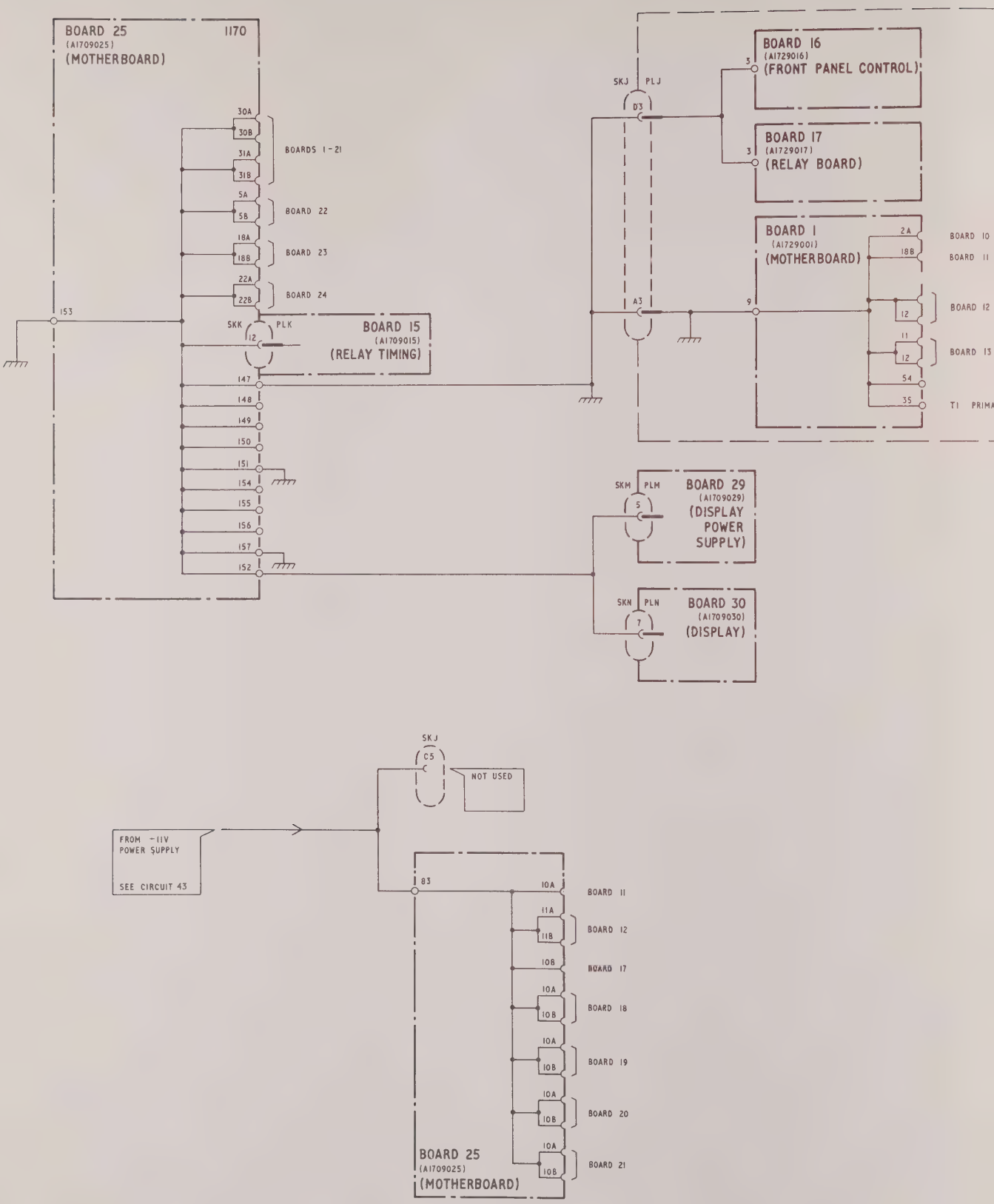

PART OF BOARD 35
(A1709035)
OF 1170
PART OF BOARD 25
(A1709025)
(MOTHERBOARD)
OF 1170
+5V (A)
3
135
C2
·1
+5V (B)
4
138
C3
·1
FROM 5V PROTECTION RELAYS
SEE CIRCUIT 43
+5V (C)
5
C4
·1
SKM
15
BOARD 29
(A1709029)
DISPLAY POWER SUPPLY
SKN
3
BOARD 30
(A1709030)
DISPLAY
+5V (D)
6
7
C5
·1
1172
BOARD 16
(A1729016)
FRONT PANEL CONTROL
2
SKJ
PLJ
A2
D2
BOARD 17
(A1729017)
RELAY BOARD
2
BOARD 1
(A1729001)
(MOTHER BOARD)
28
15
9
9
26
C13
·1
0V
BOARD 10
BOARD 11
BOARD 12
BOARD 13

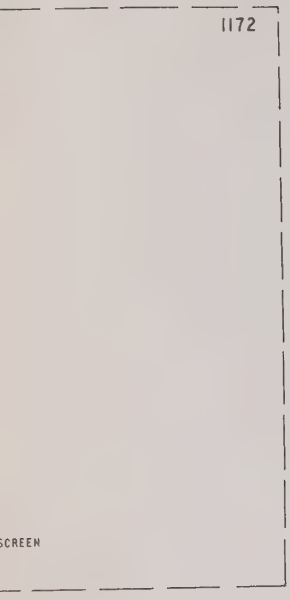

30
31
BOARD 1
BOARD 2
BOARD 3
BOARD 4
BOARD 5
136
137
NOT USED
BOARD 6
BOARD 7
BOARD 8
BOARD 9
BOARD 10
139
140
NOT USED
BOARD 11
BOARD 12
BOARD 13
BOARD 14
BOARD 15
142
143
NOT USED
BOARD 16
BOARD 17
BOARD 18
BOARD 19
BOARD 20
BOARD 21
5
BOARD 22
18
BOARD 23
22
BOARD 24
SKK
PLK
BOARD 15
(A1709015)
RELAY
TIMING
145
146
NOT USED

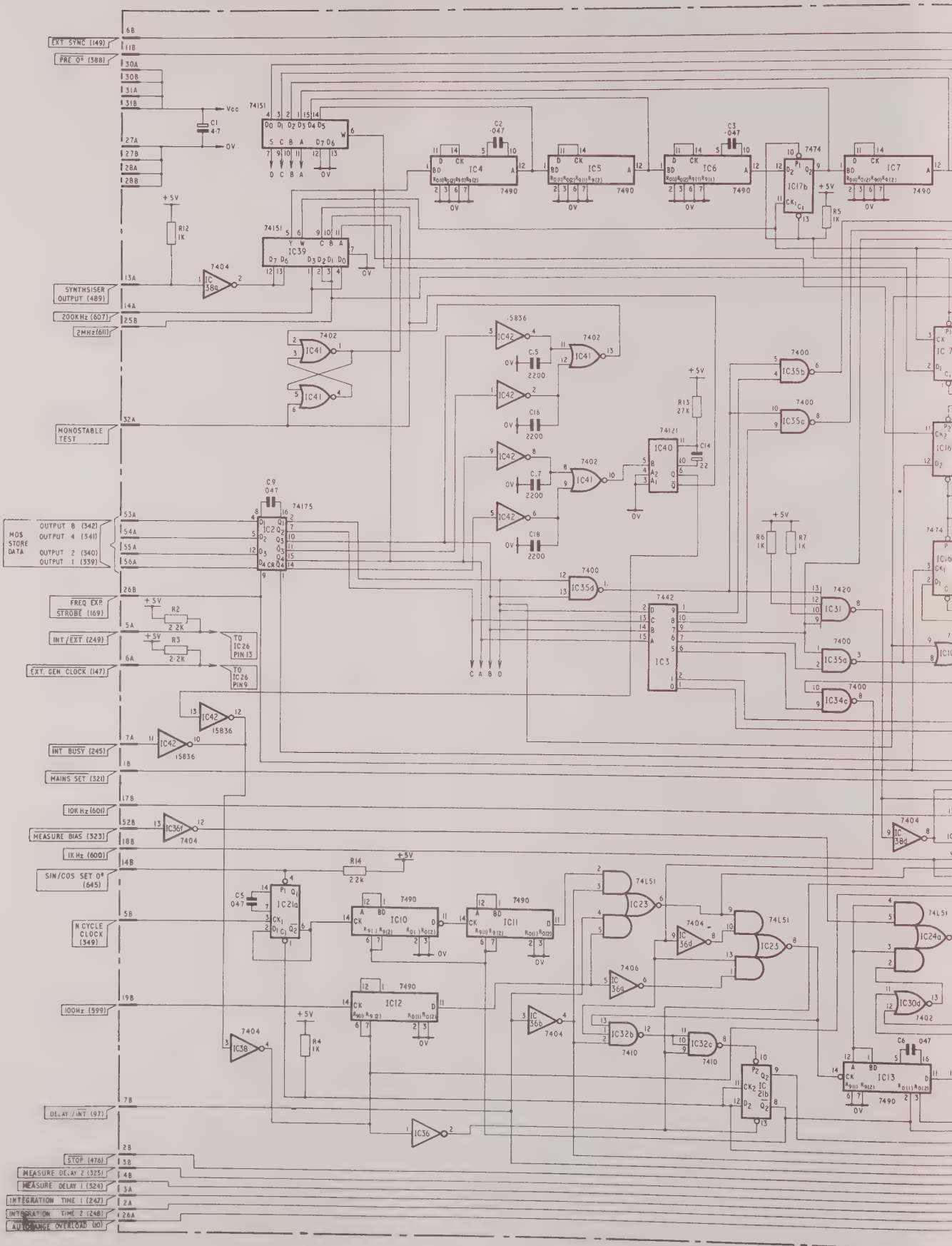

BOARD 16
(A1729016)
(FRONT PANEL CONTROL)
SKJ
PLJ
D1
BOARD 17
(A1729017)
(RELAY BOARD)
BOARD 1
(A1729001)
(MOTHER BOARD)
A1
30
PART OF BOARD 35
(A1709035)
2
1
C1
·1
+18V
FROM 18V PROTECTION RELAY
SEE CIRCUIT 43
SKL
PLL
6
7
10
BOARD 26
(A1709026)
(MAIN POWER SUPPLY)
SKM
PLM
14
BOARD 29
(A1709029)
(DISPLAY POWER SUPPLY)
BOARD 25
(A1709025)
(MOTHERBOARD)
90
1172
SKJ
PLJ
A4
3
15
15
BOARD 1
(A1729001)
(MOTHERBOARD)
BOARD 12
BOARD 13
-16V
FROM -16V POWER SUPPLY
SEE CIRCUIT 43
100
11A
11B
BOARD 18
BOARD 19
BOARD 20
BOARD 21
OPTIONAL BOARDS
BOARD 25
(A1709025)
(MOTHERBOARD)

1172
BOARD 11 (INTERFACE DRIVER)
BOARD 12 (10 MHz OSCILLATOR, MIXER & VCO)
BOARD 13 (PHASE DETECTOR)

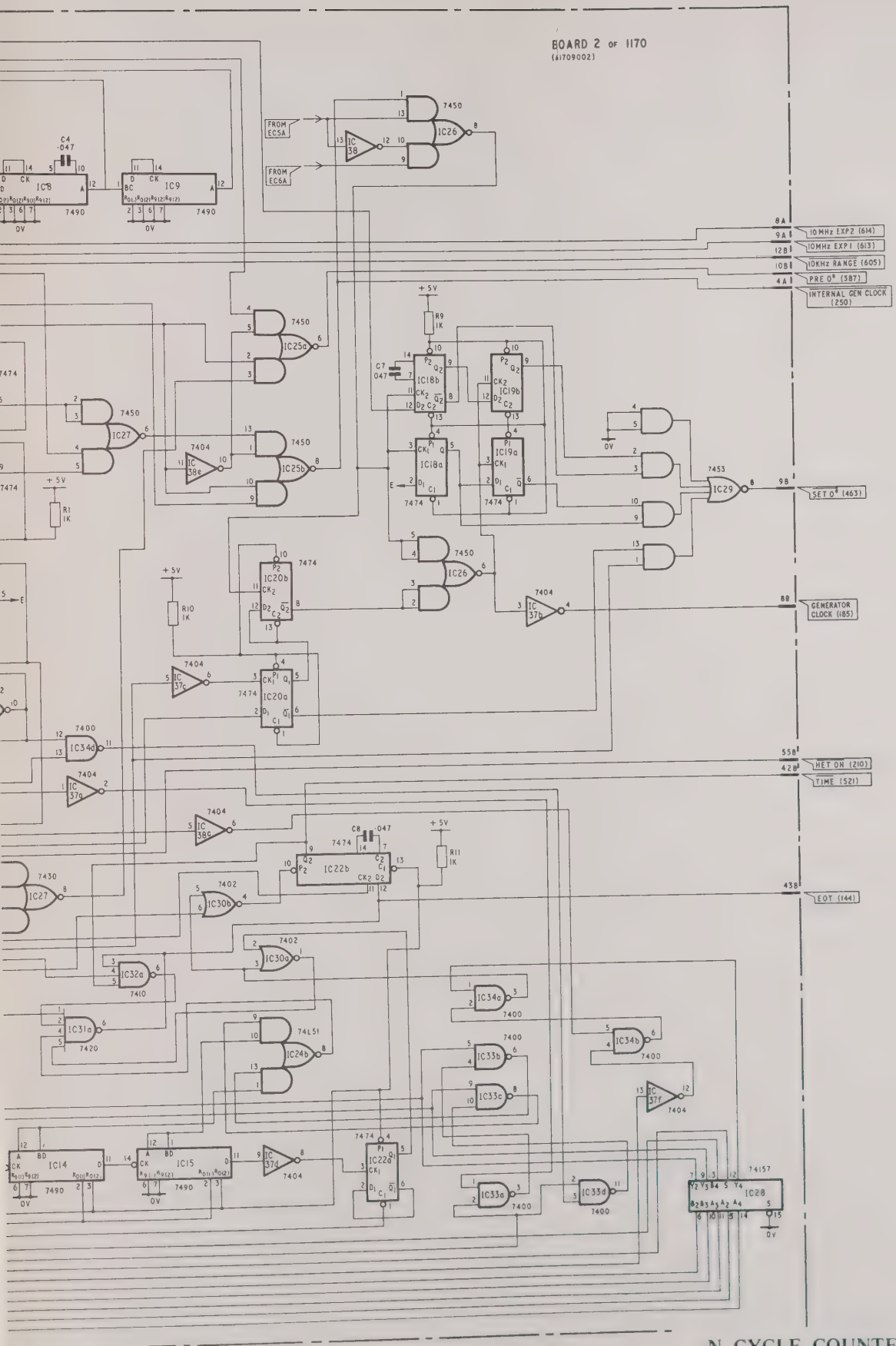

2A
12B
12A
12B
12A
12B
12A
12B
BOARD 18
BOARD 19
BOARD 20
BOARD 21
OPTIONAL BOARDS
KK
PLK
13
BOARD 15
(A1709015)
(RELAY
TIMING)


BOARD 25
(A1709025)
(MOTHERBOARD)
1170
30A
30B
31A
31B
BOARDS 1-21
5A
5B
BOARD 22
18A
18B
BOARD 23
22A
22B
BOARD 24
153
SKK
12
PLK
BOARD 15
(A1709015)
(RELAY TIMING)
147
148
149
150
151
154
155
156
157
152
SKJ
D3
PLJ
3
BOARD 16
(A1729016)
(FRONT PANEL CONTROL)
3
BOARD 17
(A1729017)
(RELAY BOARD)
A3
9
BOARD 1
(A1729001)
(MOTHERBOARD)
2A
18B
BOARD 10
BOARD 11
12
BOARD 12
11
12
BOARD 13
54
35
T1 PRIMA
SKM
5
PLM
BOARD 29
(A1709029)
(DISPLAY POWER SUPPLY)
SKN
7
PLN
BOARD 30
(A1709030)
(DISPLAY)
SKJ
C5
NOT USED
FROM -11V POWER SUPPLY
SEE CIRCUIT 43
83
10A
BOARD 11
11A
11B
BOARD 12
10B
BOARD 17
10A
10B
BOARD 18
10A
10B
BOARD 19
10A
10B
BOARD 20
10A
10B
BOARD 21
BOARD 25
(A1709025)
(MOTHERBOARD)


1172
SCREEN

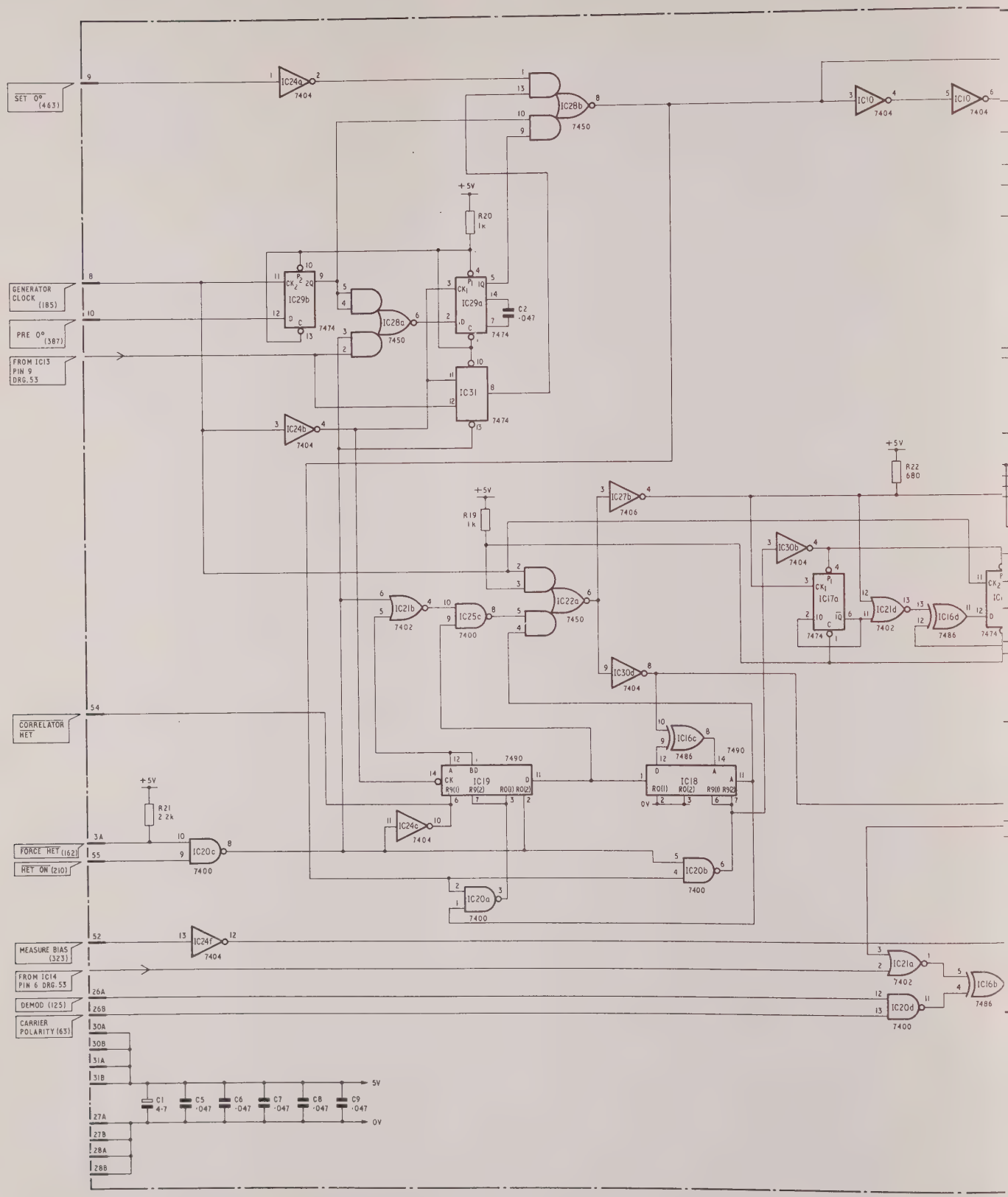


SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

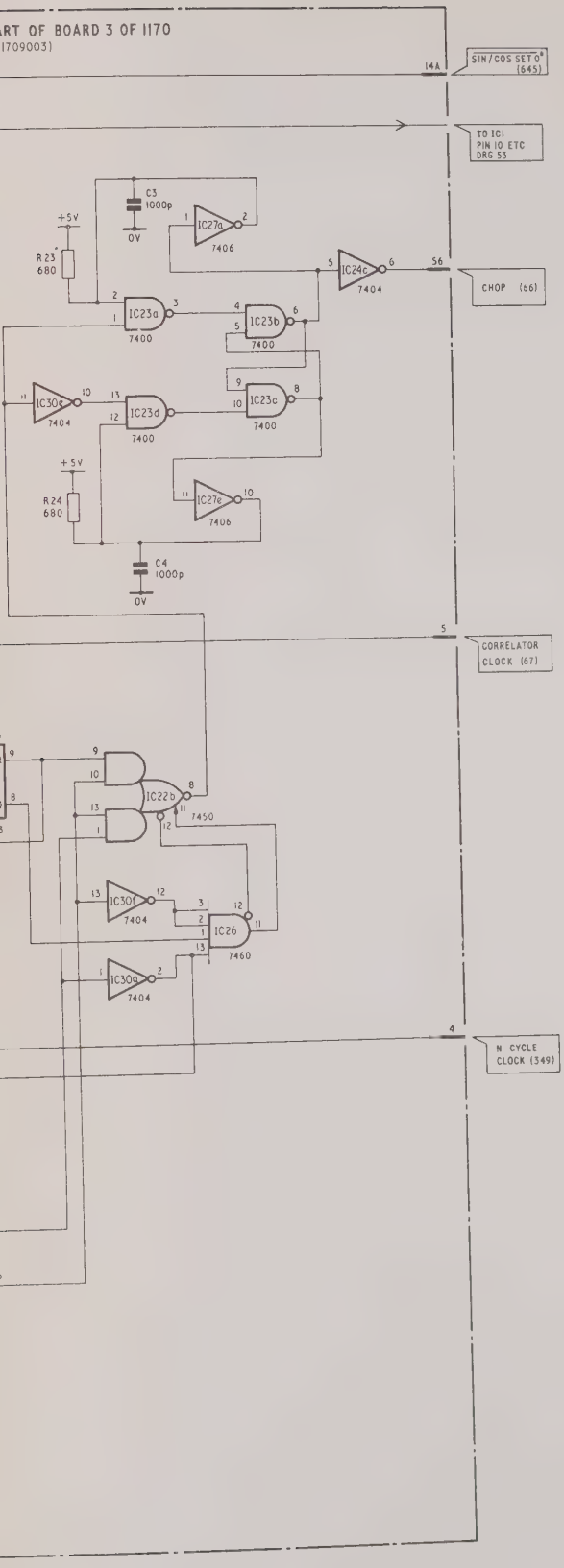


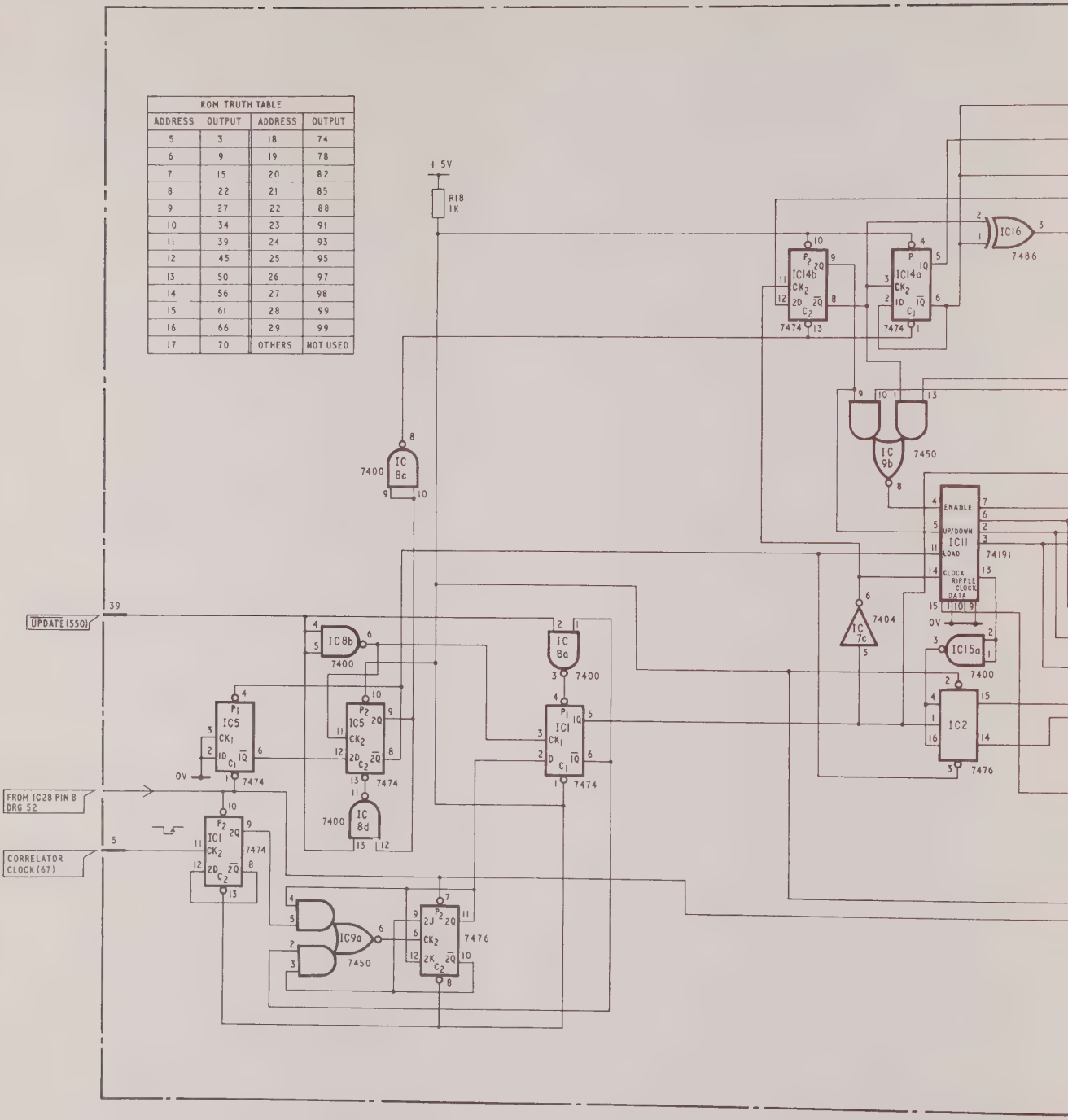
N CYCLE COUNTER AND GENERATOR DIVIDER

D11707050-02

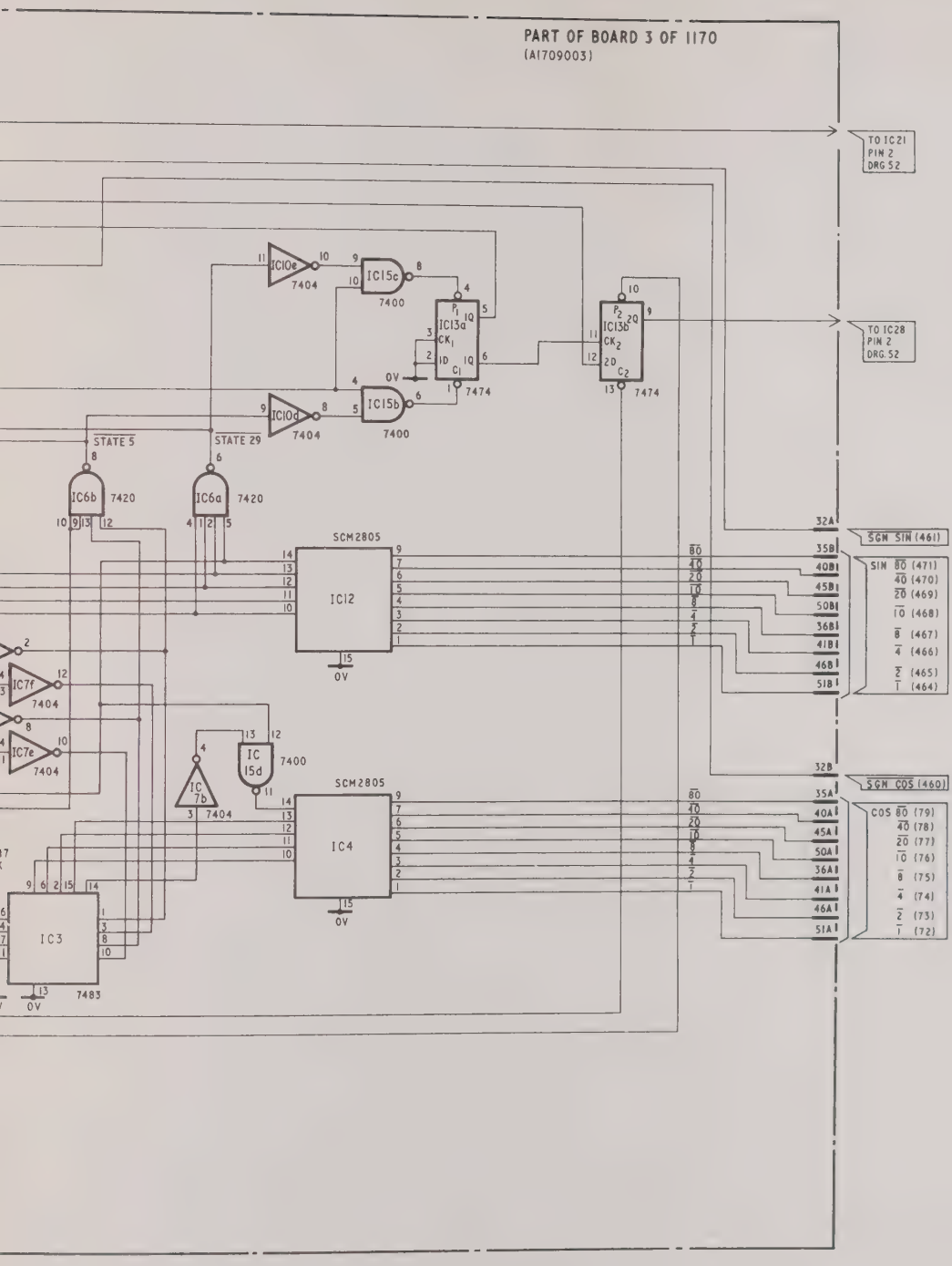


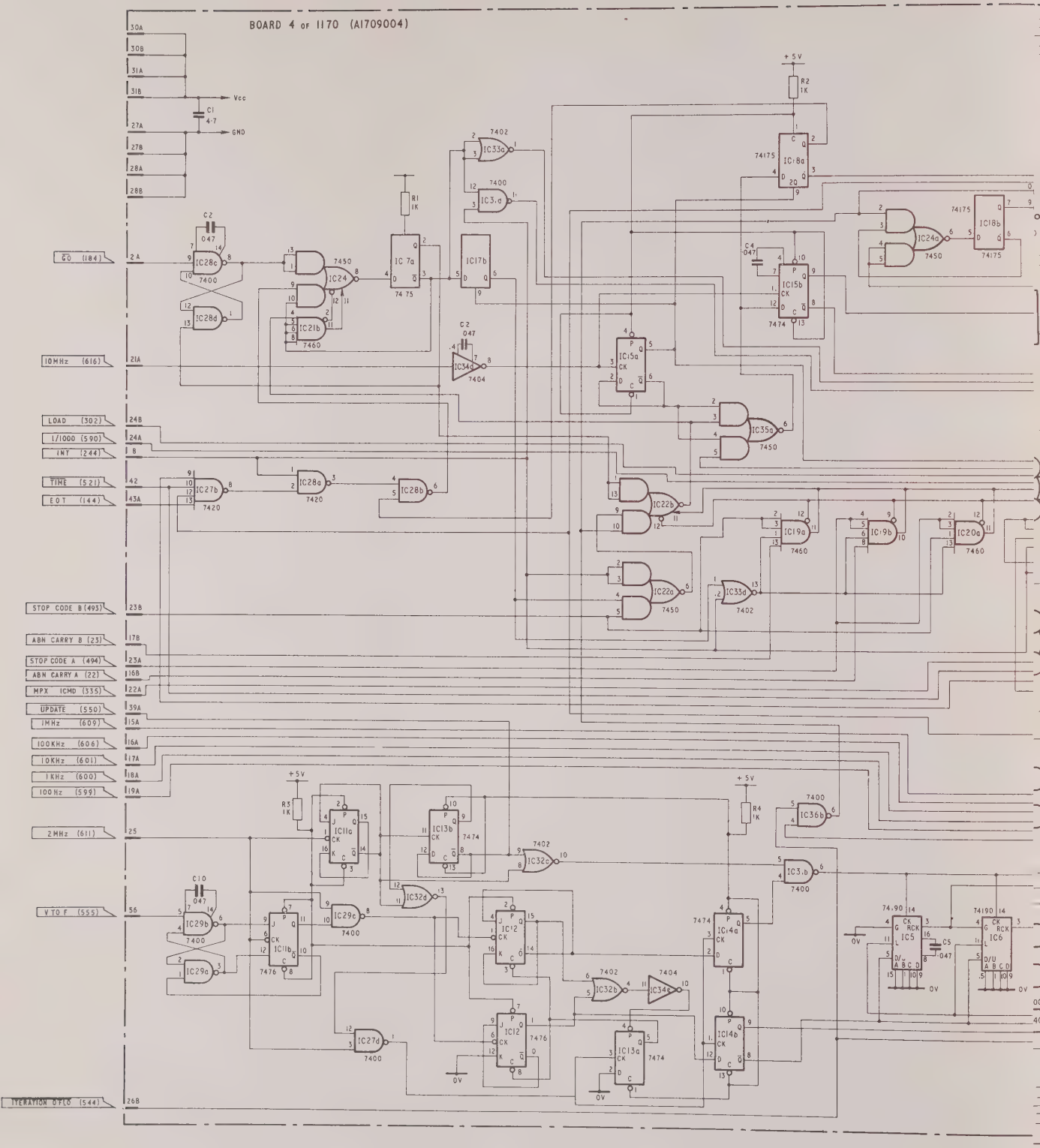
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


ART OF BOARD 3 OF 1170
(1709003)
14A
SIN/COS SET 0°
(645)
TO IC1
PIN 10 ETC
DRG 53
C3
1000p
0V
+5V
R23
680
IC27a
7406
IC24c
7404
56
CHOP (66)
IC23a
IC23b
7400
IC30e
7404
IC23d
IC23c
7400
+5V
R24
680
IC27e
7406
C4
1000p
0V
5
CORRELATOR
CLOCK (67)
IC22b
7450
IC30f
7404
IC26
7460
IC30g
7404
4
N CYCLE
CLOCK (349)

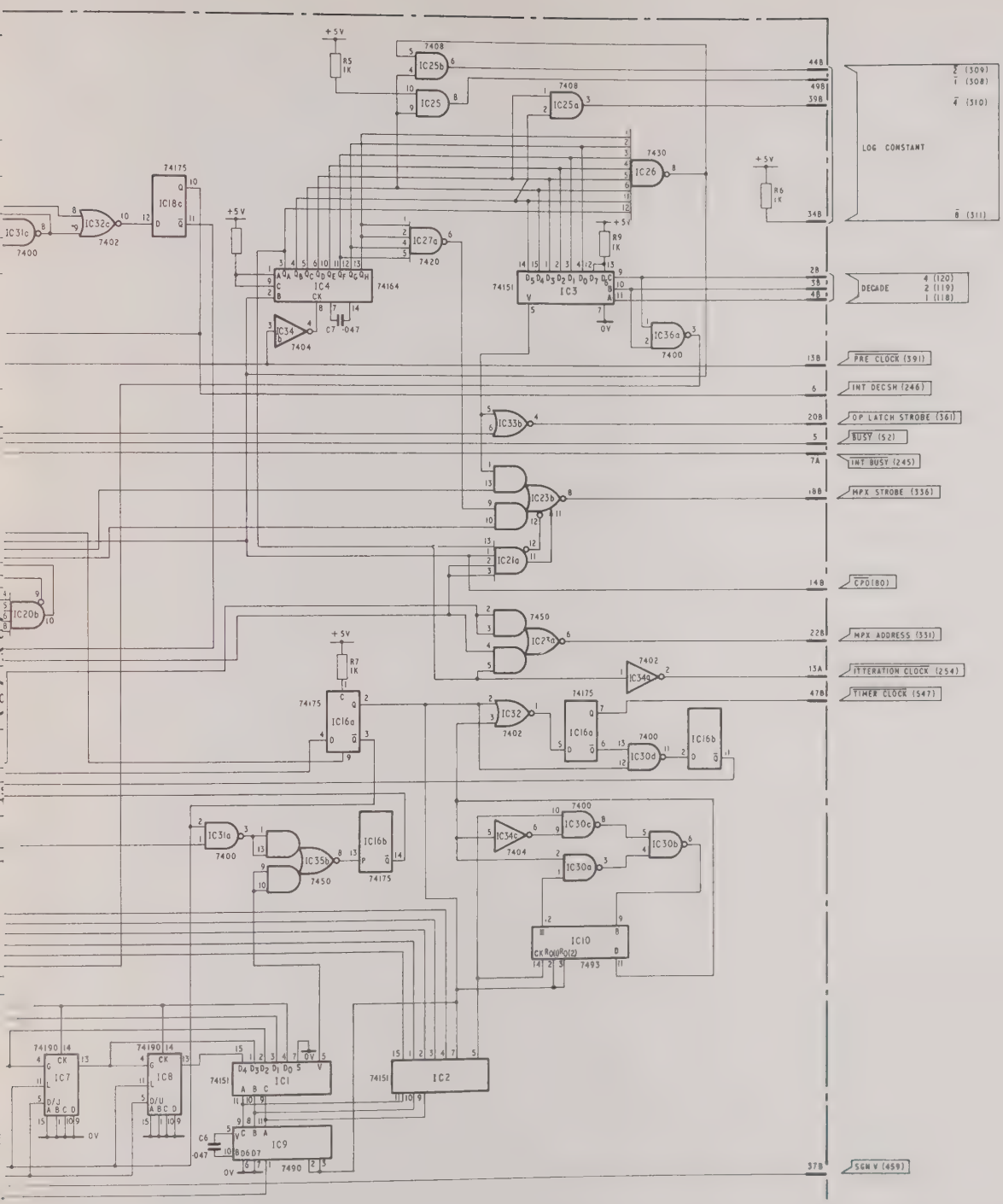


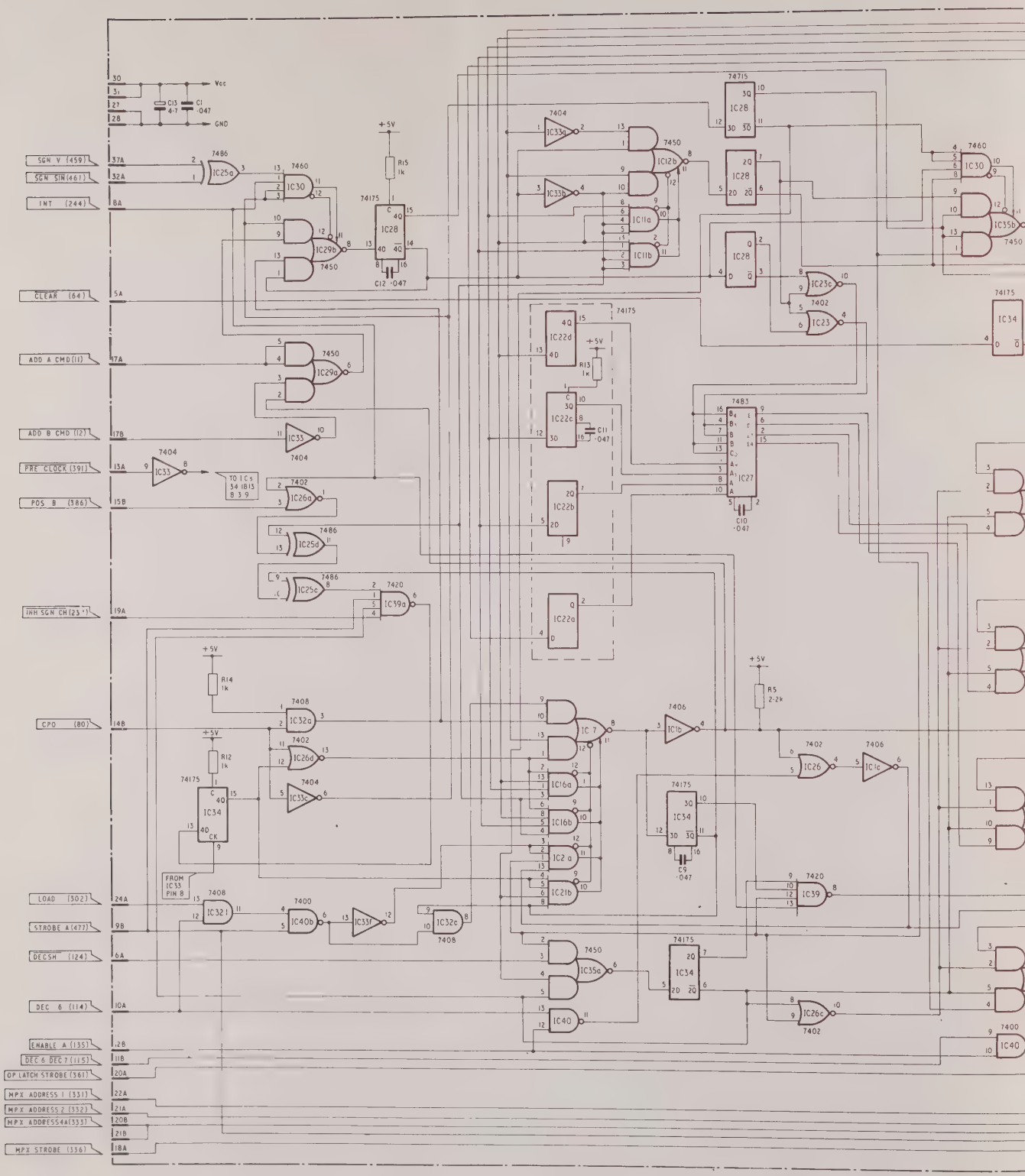
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


PART OF BOARD 3 OF 1170
(A1709003)
TO IC21 PIN 2 DRG 52
TO IC28 PIN 2 DRG 52
IC10e 7404
IC15c 7400
IC13a 7474
IC13b 7474
IC10d 7404
IC15b 7400
0V
STATE 5
STATE 29
IC6b 7420
IC6a 7420
SCM2805
IC12
IC7f 7404
IC7e 7404
IC 15d 7400
IC 7b 7404
SCM2805
IC4
IC3 7483
32A
SGN SIN (461)
35B
40B
45B
50B
36B
41B
46B
51B
SIN 80 (471)
40 (470)
20 (469)
10 (468)
8 (467)
4 (466)
2 (465)
1 (464)
32B
SGN COS (460)
35A
40A
45A
50A
36A
41A
46A
51A
COS 80 (79)
40 (78)
20 (77)
10 (76)
8 (75)
4 (74)
2 (73)
1 (72)

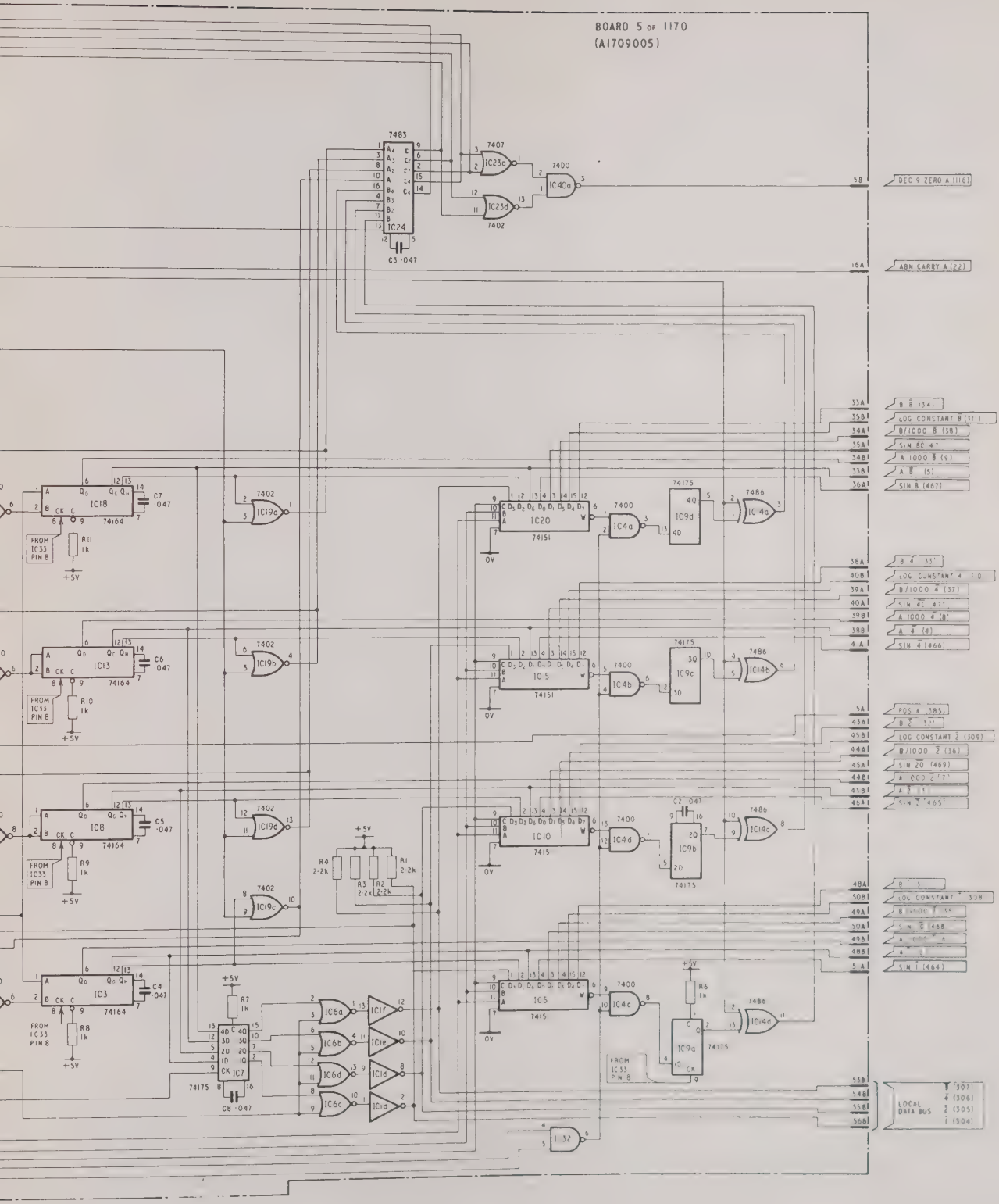


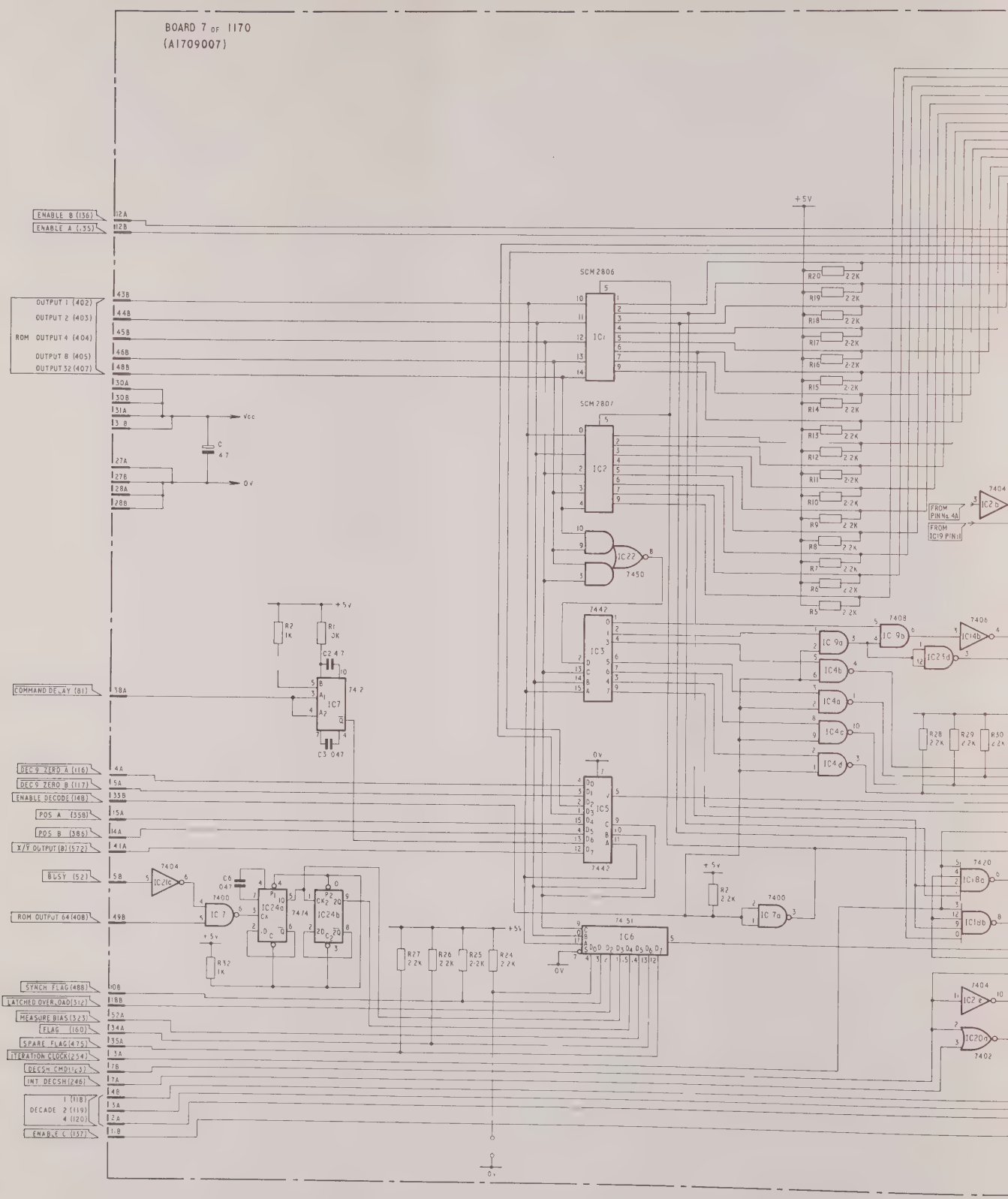
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


LOG CONSTANT
DECADE
4 (120)
2 (119)
1 (118)
PRE CLOCK (391)
INT DECSH (246)
OP LATCH STROBE (361)
BUSY (52)
INT BUSY (245)
MPX STROBE (336)
CPO (80)
MPX ADDRESS (331)
ITTERATION CLOCK (254)
TIMER CLOCK (547)
SGN V (459)
IC1
IC2
IC3
IC4
IC7
IC8
IC9
IC10
IC16a
IC16b
IC18c
IC20b
IC21a
IC23b
IC25
IC25a
IC25b
IC26
IC27a
IC27b
IC30a
IC30b
IC30c
IC30d
IC31a
IC31c
IC32
IC32c
IC33b
IC34a
IC34c
IC35b
IC36a
74164
74175
74190
74151
7493
7490
7400
7402
7404
7408
7420
7430
7450

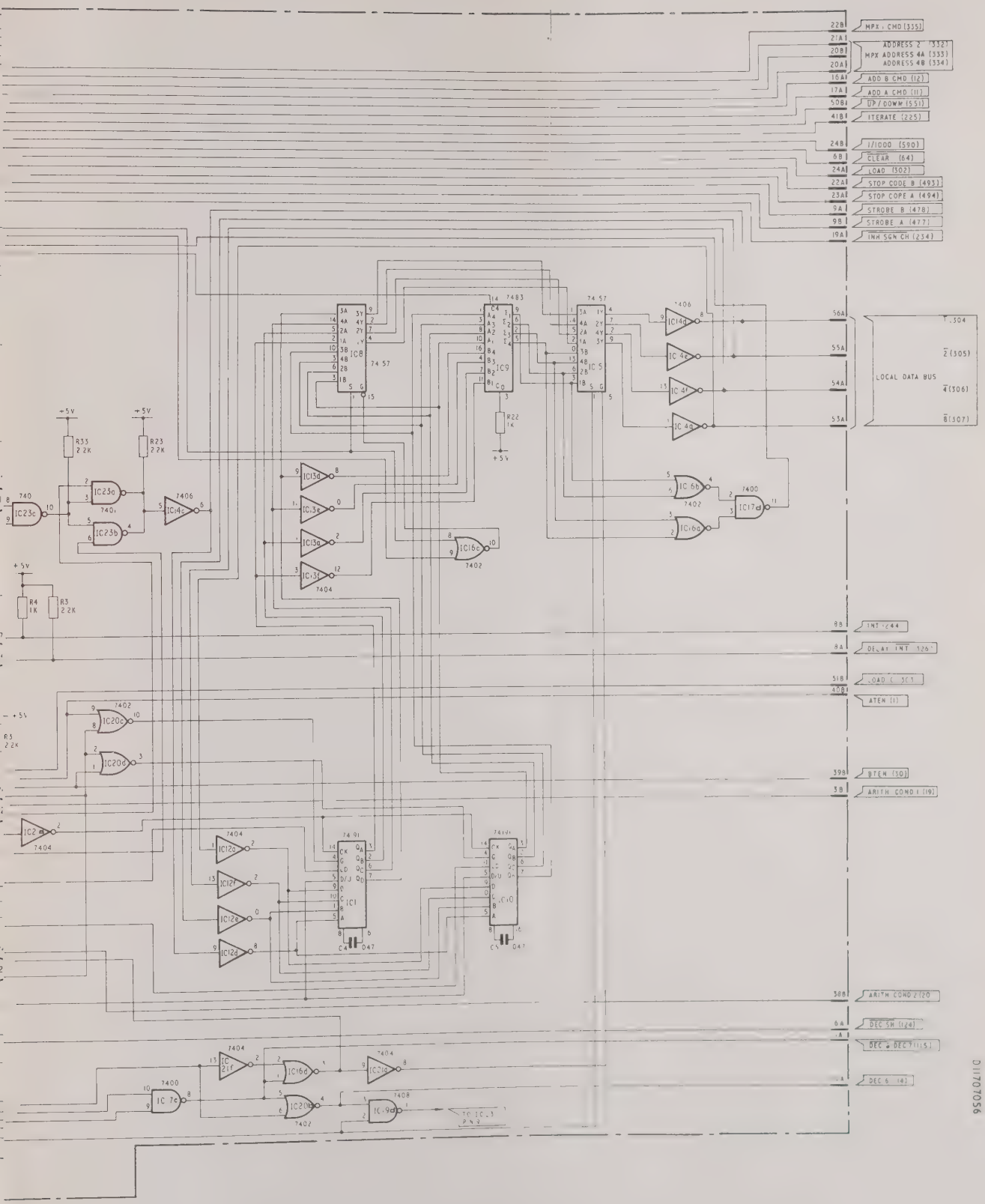


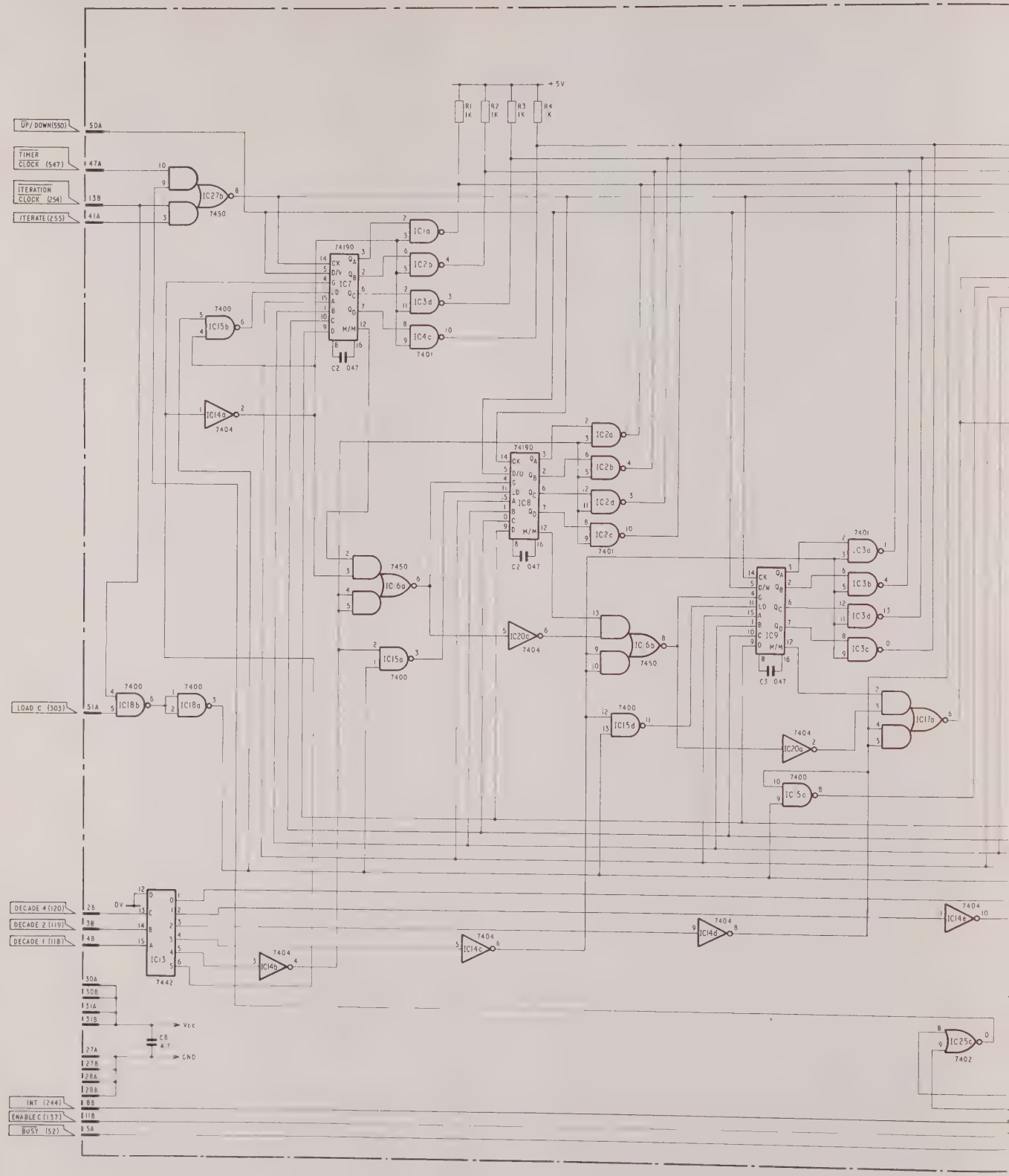
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


BOARD 5 OF 1170
(A1709005)
7483
IC24
C3 ·047
7407
IC23a
7400
IC40a
IC23d
7402
5B
DEC 9 ZERO A (116)
16A
ABN CARRY A (22)
33A
35B
54A
35A
34B
53B
36A
38A
40B
39A
40A
39B
4 A
58A
5A
43A
45B
44A
45A
44B
43B
46A
48A
50B
49A
50A
49B
48B
5 A
55B
54B
55B
56B
LOCAL DATA BUS
IC18
IC13
IC8
IC3
74164
C7 ·047
C6 ·047
C5 ·047
C4 ·047
R11 1k
R10 1k
R9 1k
R8 1k
FROM IC33 PIN 8
+5V
7402
IC19a
IC19b
IC19d
IC19c
IC20
IC5
IC10
74151
7400
IC4a
IC4b
IC4d
IC4c
74175
IC9d
IC9c
IC9b
IC9a
7486
IC14a
IC14b
IC14c
IC14d
0V
C2 ·047
R4 2-2k
R3 2-2k
R2 2-2k
R1 2-2k
R7 1k
R6 1k
IC7
IC6a
IC6b
IC6d
IC6c
IC1f
IC1e
IC1d
IC1a
C8 ·047
1-32

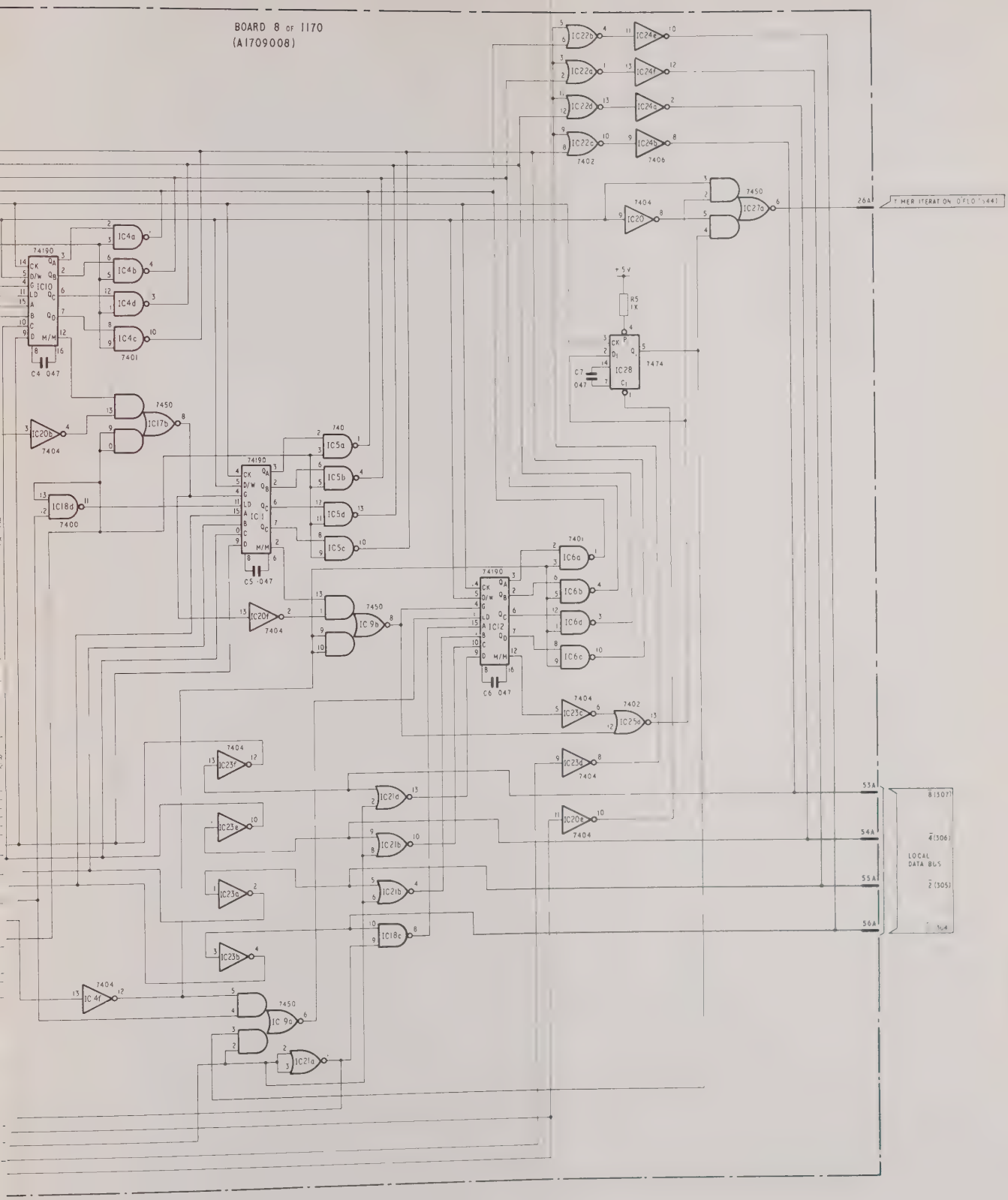


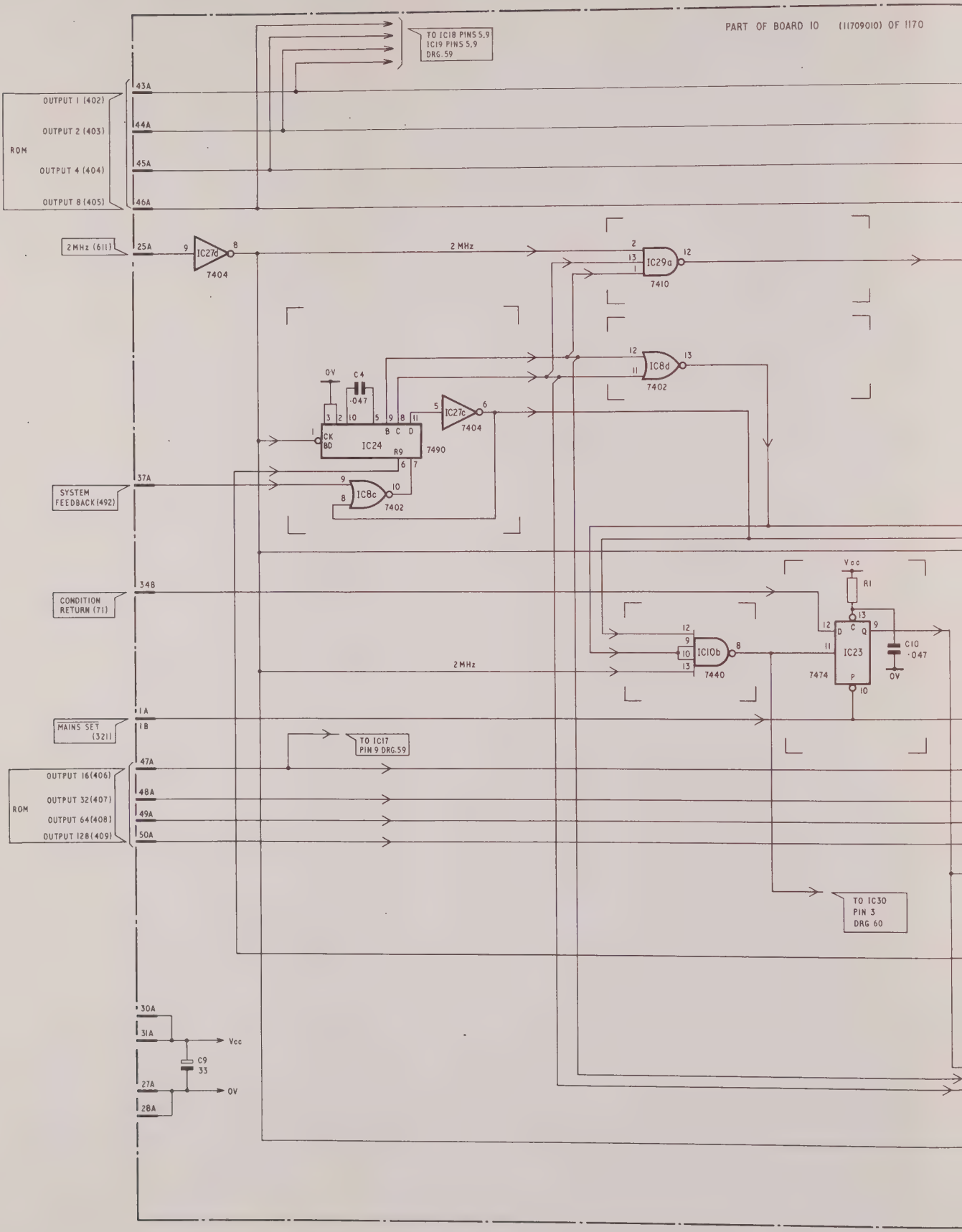
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


MPX ↓ CMD (335)
ADDRESS 2 (332)
MPX ADDRESS 4A (333)
ADDRESS 4B (334)
ADD B CMD (12)
ADD A CMD (11)
UP / DOWN (551)
ITERATE (225)
1/1000 (590)
CLEAR (64)
LOAD (302)
STOP CODE B (493)
STOP CODE A (494)
STROBE B (478)
STROBE A (477)
INH SGN CH (234)
LOCAL DATA BUS
INT (244)
DELAY INT (326)
ATEN (1)
BTEN (30)
ARITH COND 1 (19)
ARITH COND 2 (20)
DEC SM (124)
DEC 6 (42)
+5V
R33 2.2K
R23 2.2K
R4 1K
R3 2.2K
R22 1K
7400
7402
7404
7406
7408
7410
7427
7483
7491
74157
D11707056

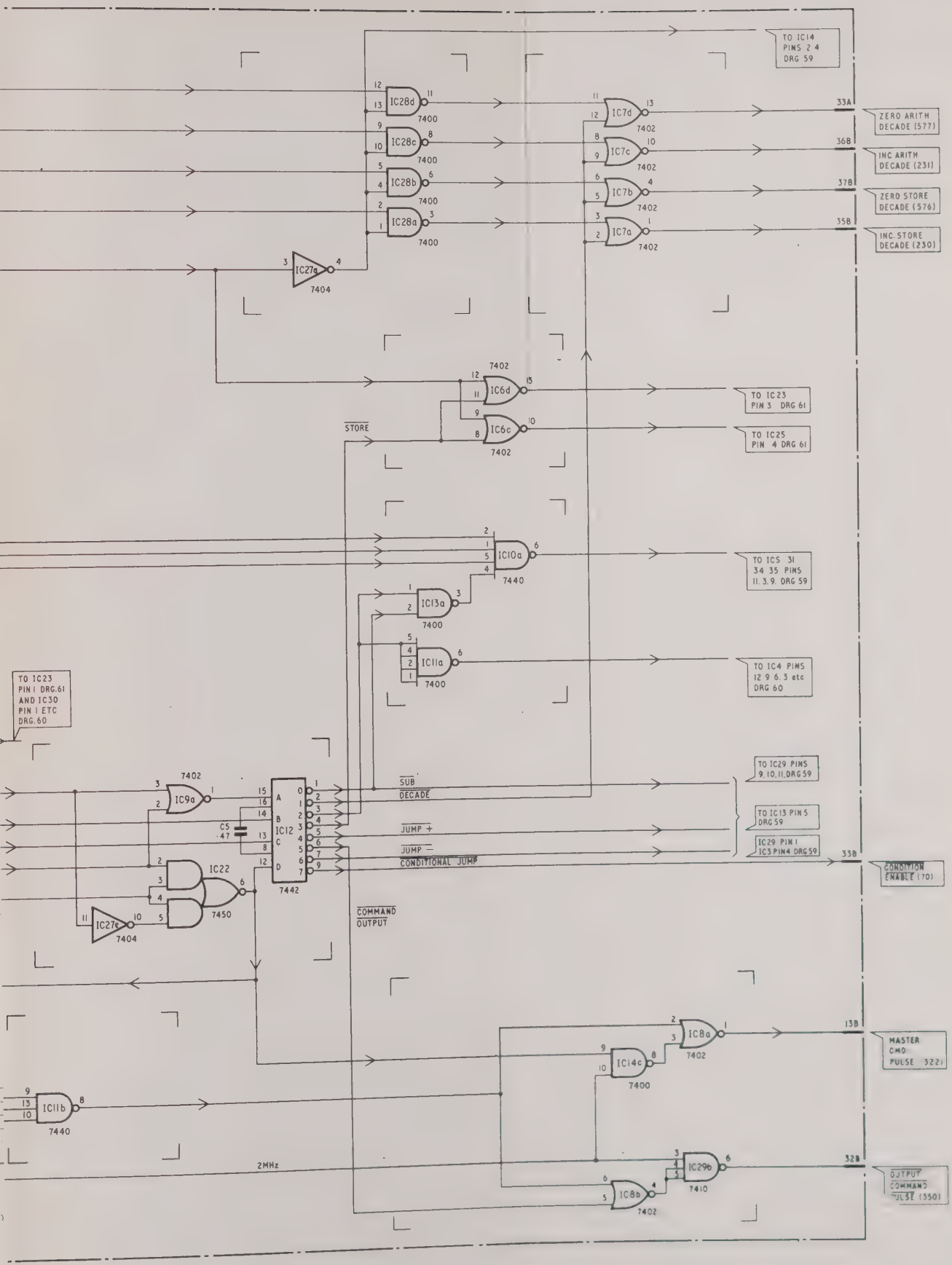


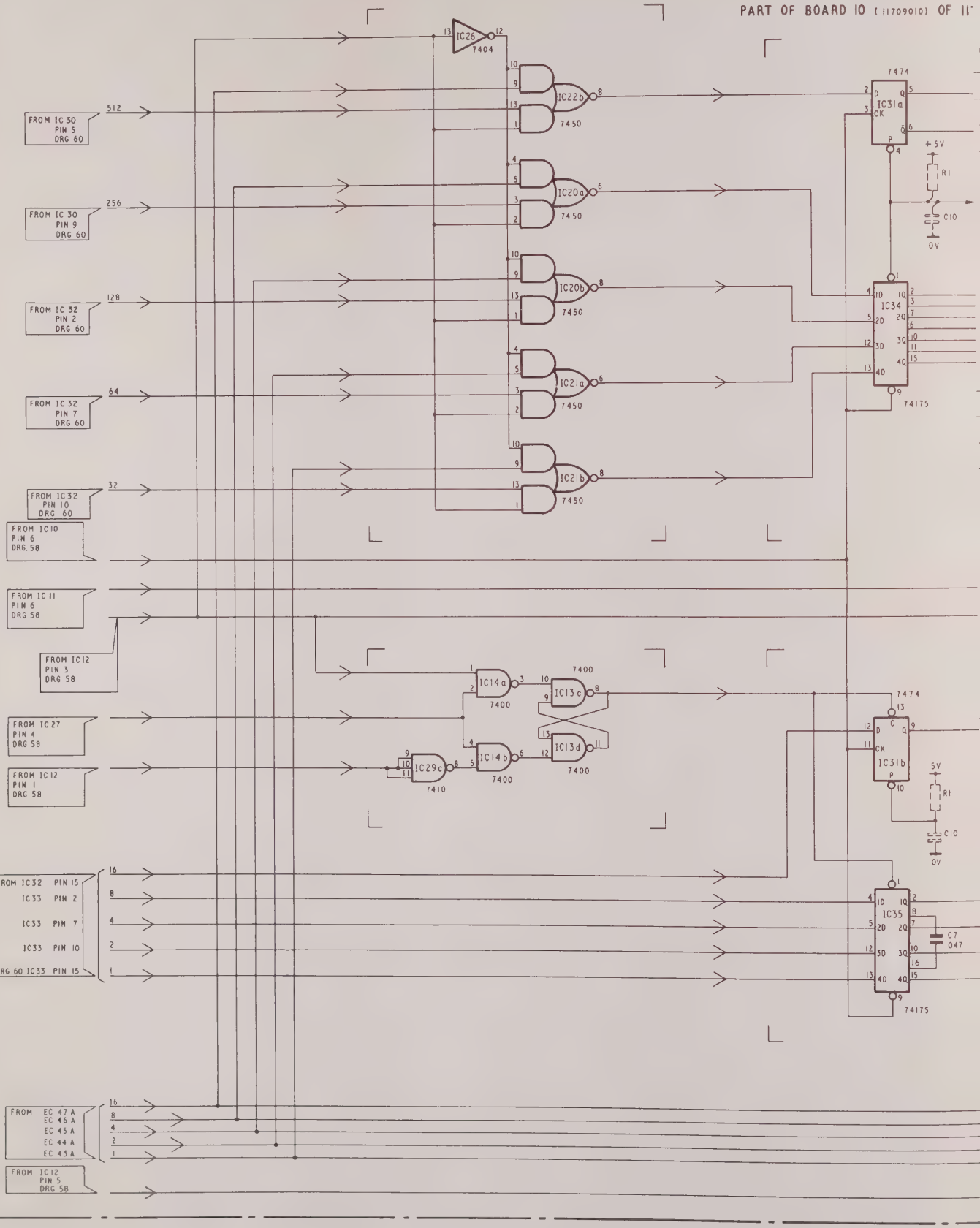
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTI


BOARD 8 OF 1170
(A1709008)
74190
7401
7450
7404
7400
740
7402
7406
74LS41
7474
+5V
R5
1K
C4 047
C5 047
C6 047
C7
047
26A
53A
54A
55A
56A
LOCAL
DATA BUS
D11707057

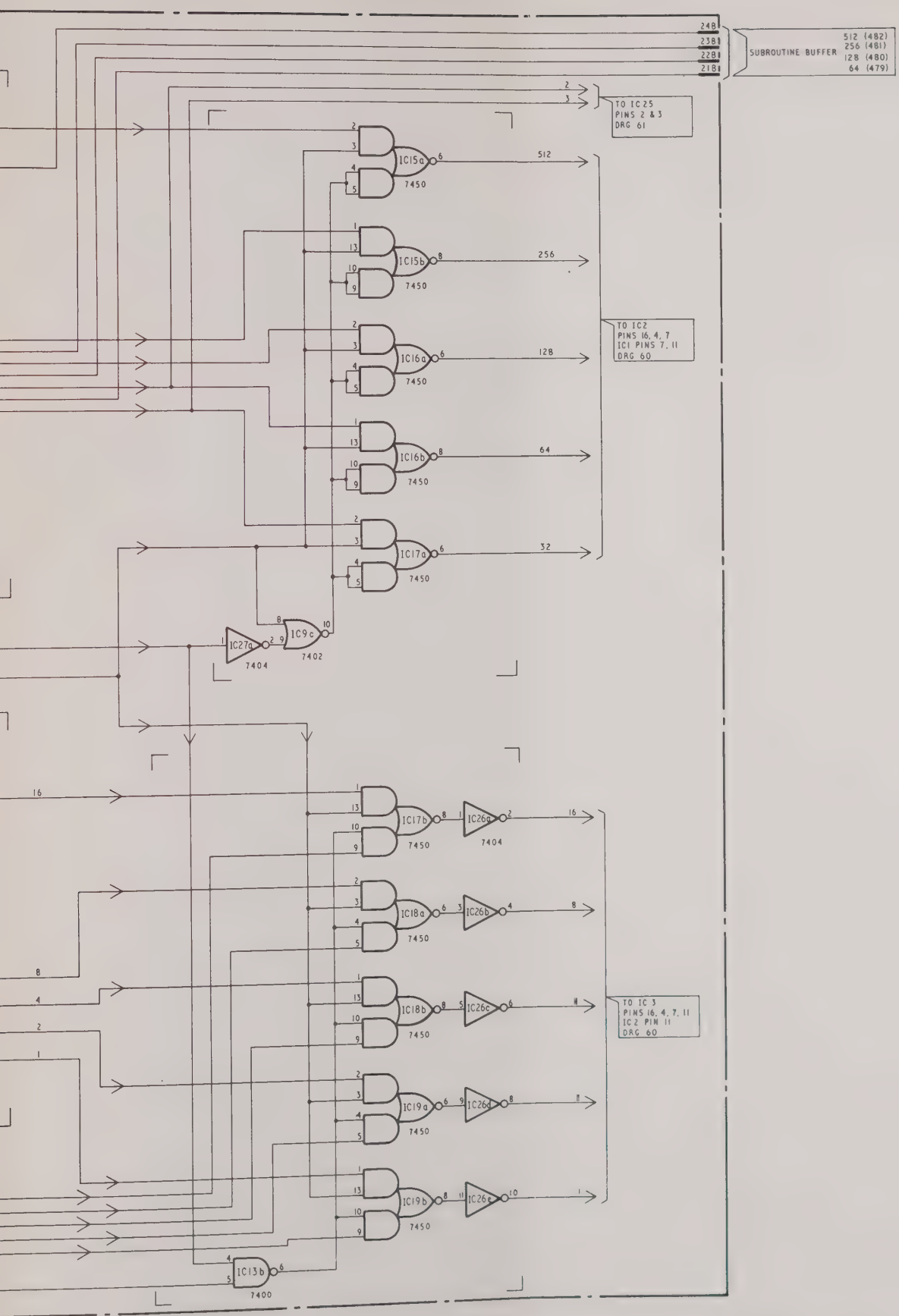


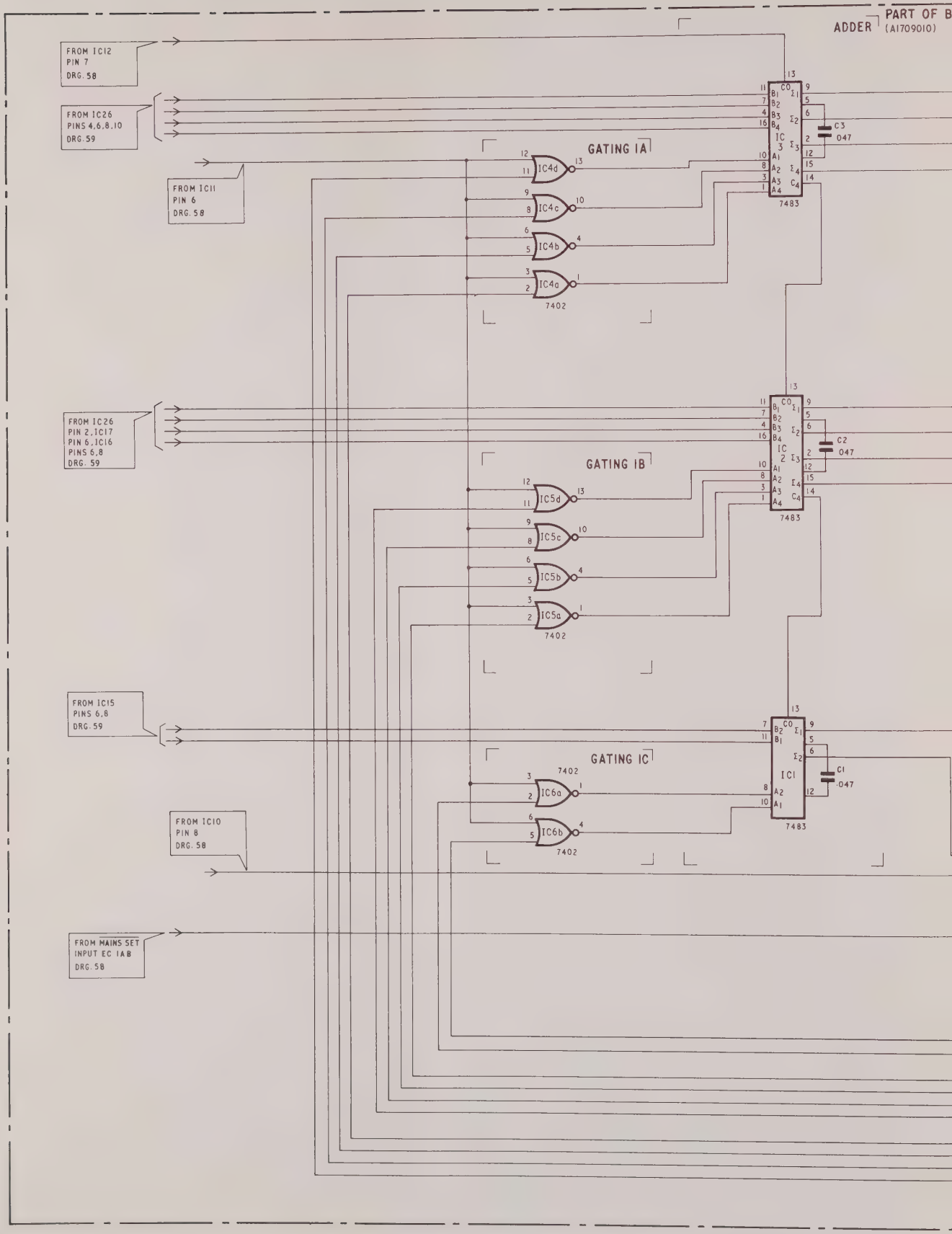
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 3


TO IC14 PINS 2 4 DRG 59
IC28d
IC28c
IC28b
IC28a
7400
IC27a
7404
IC7d
IC7c
IC7b
IC7a
7402
33A
ZERO ARITH DECADE (577)
36B
INC ARITH DECADE (231)
37B
ZERO STORE DECADE (576)
35B
INC. STORE DECADE (230)
IC6d
IC6c
7402
STORE
TO IC23 PIN 3 DRG 61
TO IC25 PIN 4 DRG 61
IC10a
7440
IC13a
7400
IC11a
7400
TO ICS 31 34 35 PINS 11. 3. 9. DRG 59
TO IC4 PINS 12 9 6. 3 etc DRG 60
TO IC23 PIN 1 DRG.61 AND IC30 PIN 1 ETC DRG.60
IC9a
7402
C5 .47
IC12
7442
IC22
7450
IC27c
7404
SUB DECADE
JUMP +
JUMP −
CONDITIONAL JUMP
TO IC29 PINS 9,10,11, DRG 59
TO IC13 PIN 5 DRG 59
IC29 PIN 1 IC3 PIN 4 DRG 59
33B
CONDITION ENABLE (70)
COMMAND OUTPUT
IC8a
IC14c
7402
7400
13B
MASTER CMD PULSE 322)
IC11b
7440
2MHz
IC29b
7410
IC8b
7402
32B
OUTPUT COMMAND PULSE (350)

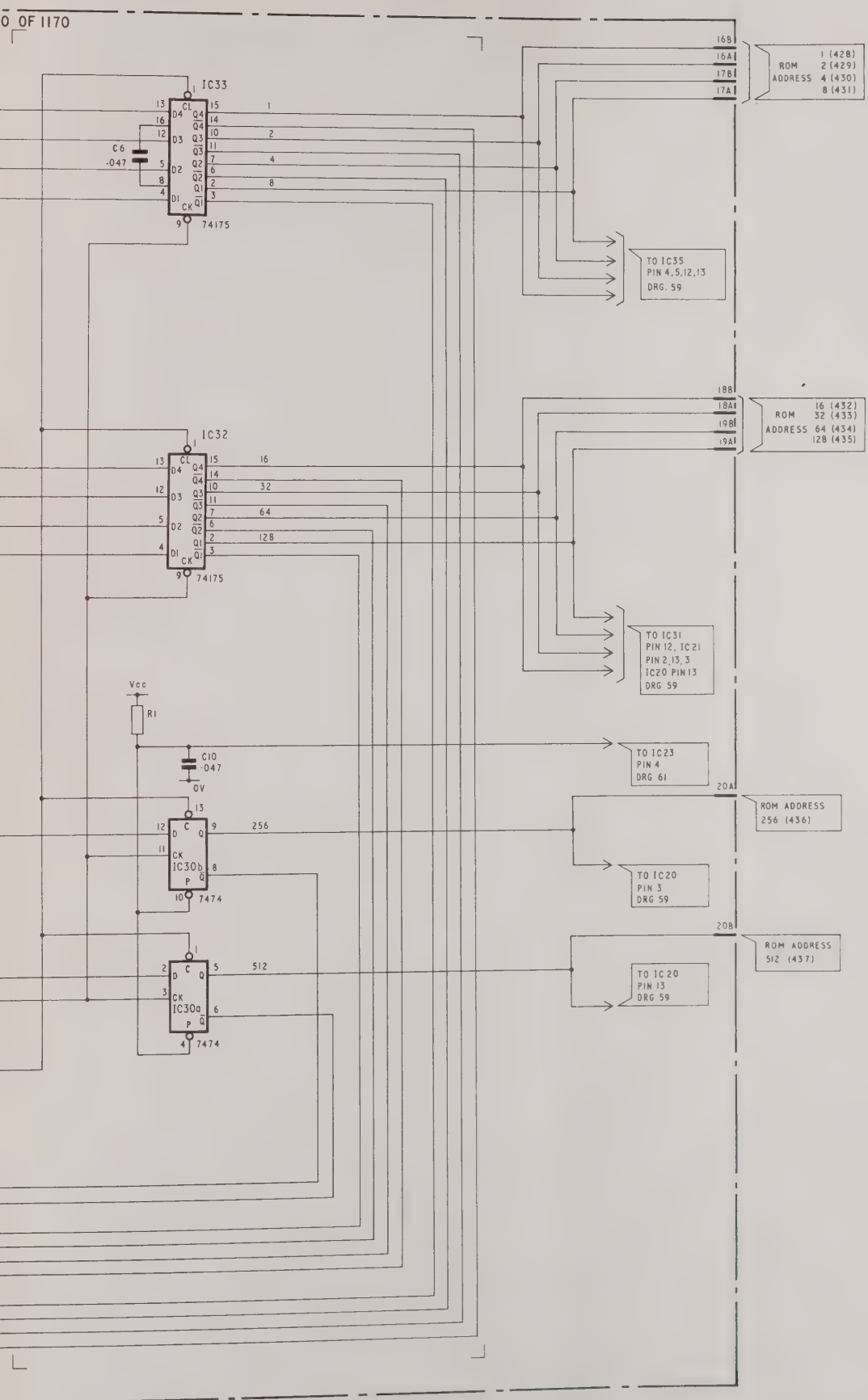


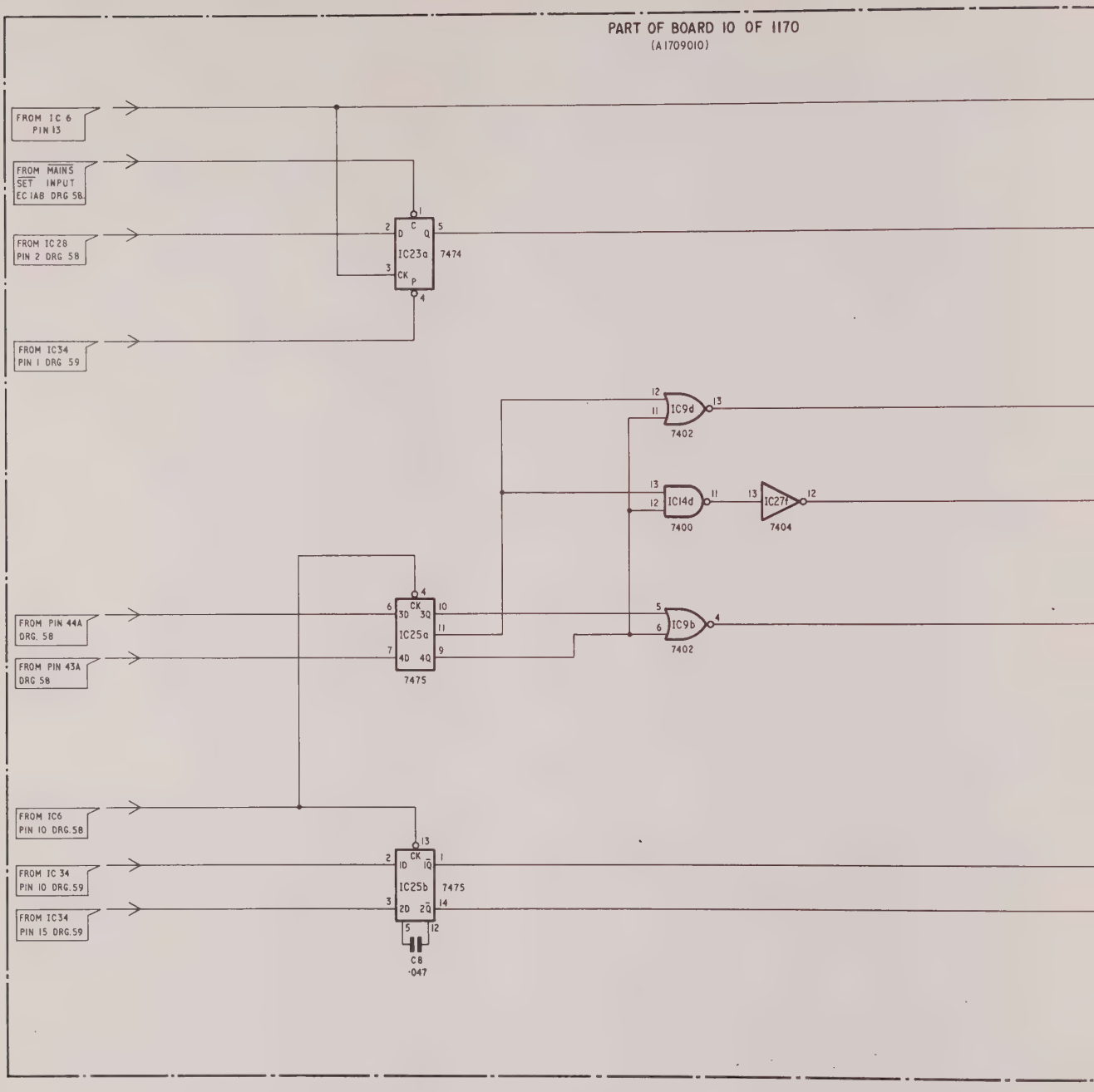
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


248
238
228
218
SUBROUTINE BUFFER
512 (482)
256 (481)
128 (480)
64 (479)
TO IC 25
PINS 2 & 3
DRG 61
IC15a
7450
512
IC15b
7450
256
TO IC2
PINS 16, 4, 7
IC1 PINS 7, 11
DRG 60
IC16a
7450
128
IC16b
7450
64
IC17a
7450
32
IC27a
7404
IC9c
7402
IC17b
7450
IC26a
7404
16
IC18a
7450
IC26b
8
IC18b
7450
IC26c
TO IC 3
PINS 16, 4, 7, 11
IC 2 PIN 11
DRG 60
IC19a
7450
IC26d
IC19b
7450
IC26e
1
IC13b
7400



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


0 OF 1170
IC33
74175
C6
.047
1
2
4
8
16B
16A
17B
17A
ROM ADDRESS
1 (428)
2 (429)
4 (430)
8 (431)
TO IC35
PIN 4,5,12,13
DRG. 59
IC32
74175
16
32
64
128
18B
18A
19B
19A
ROM ADDRESS
16 (432)
32 (433)
64 (434)
128 (435)
TO IC31
PIN 12, IC21
PIN 2,13,3
IC20 PIN 13
DRG 59
Vcc
R1
C10
.047
0V
TO IC23
PIN 4
DRG 61
IC30b
7474
256
20A
ROM ADDRESS
256 (436)
TO IC20
PIN 3
DRG 59
IC30a
7474
512
20B
ROM ADDRESS
512 (437)
TO IC20
PIN 13
DRG 59



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

STORE COMMAND PULSE (491)

ENABLE STORE (138)

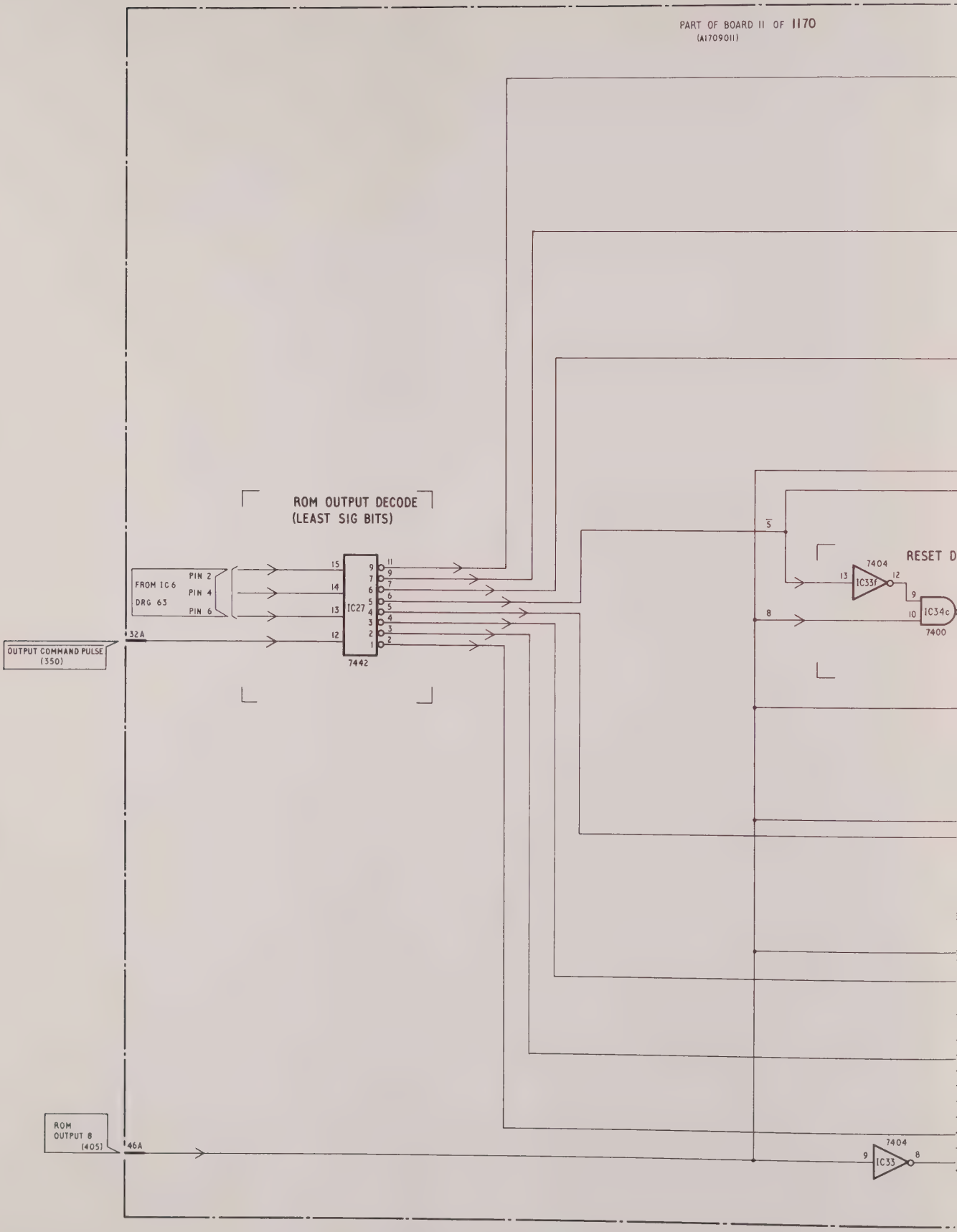
ENABLE A (135)

ENABLE B (136)

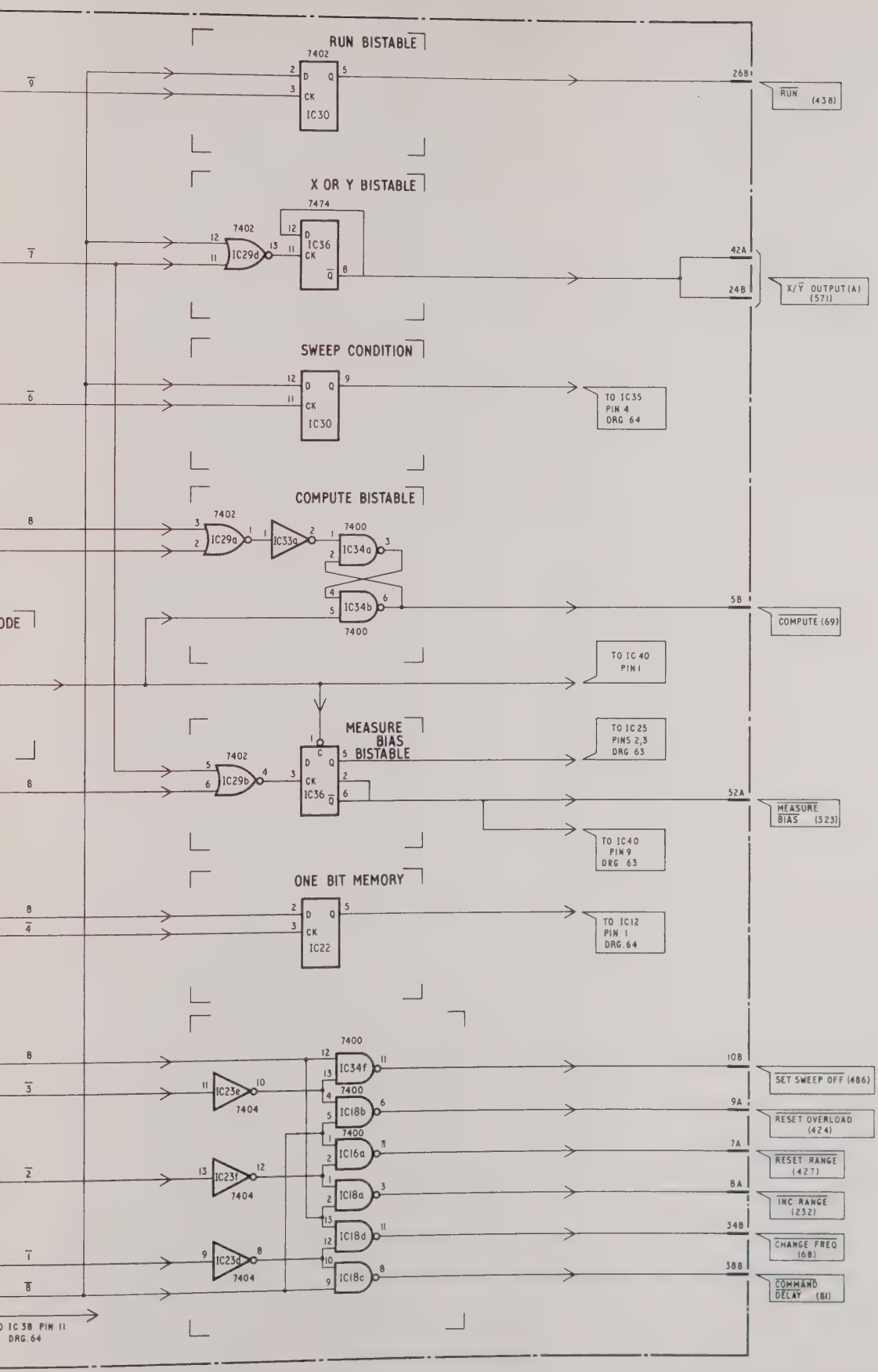
ENABLE C (137)

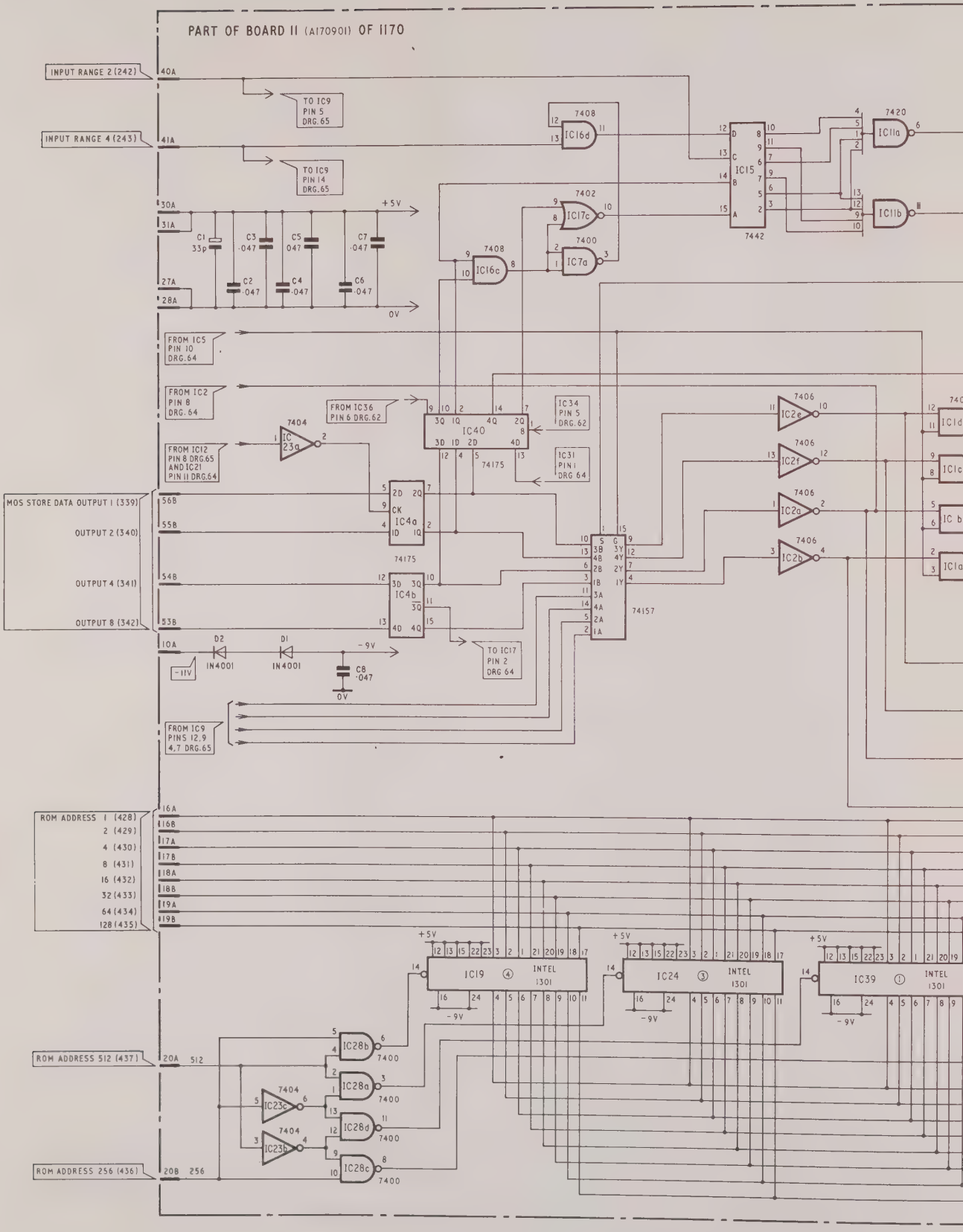
STORE ADDRESS 16 (495)

STORE ADDRESS 8 (496)

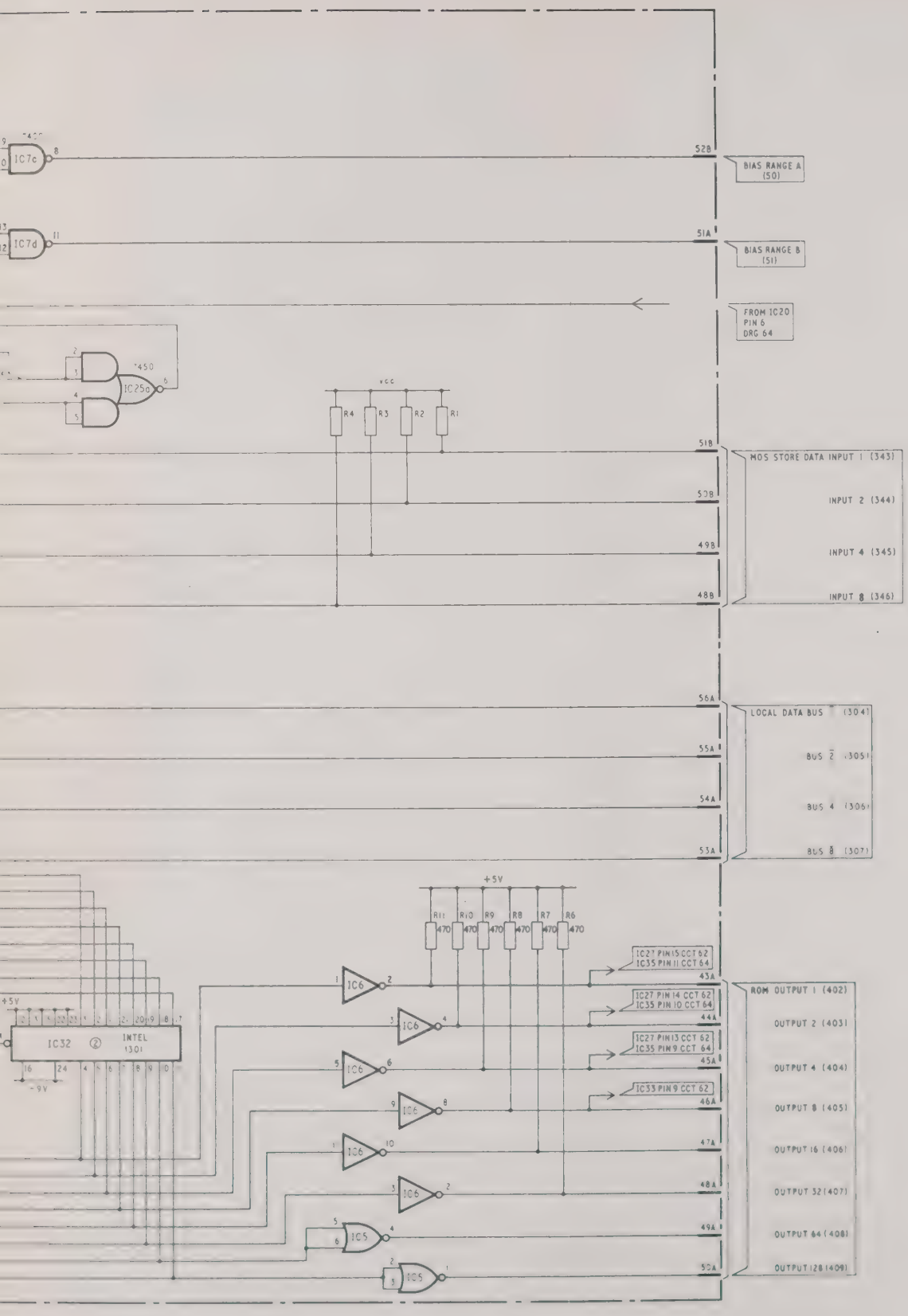


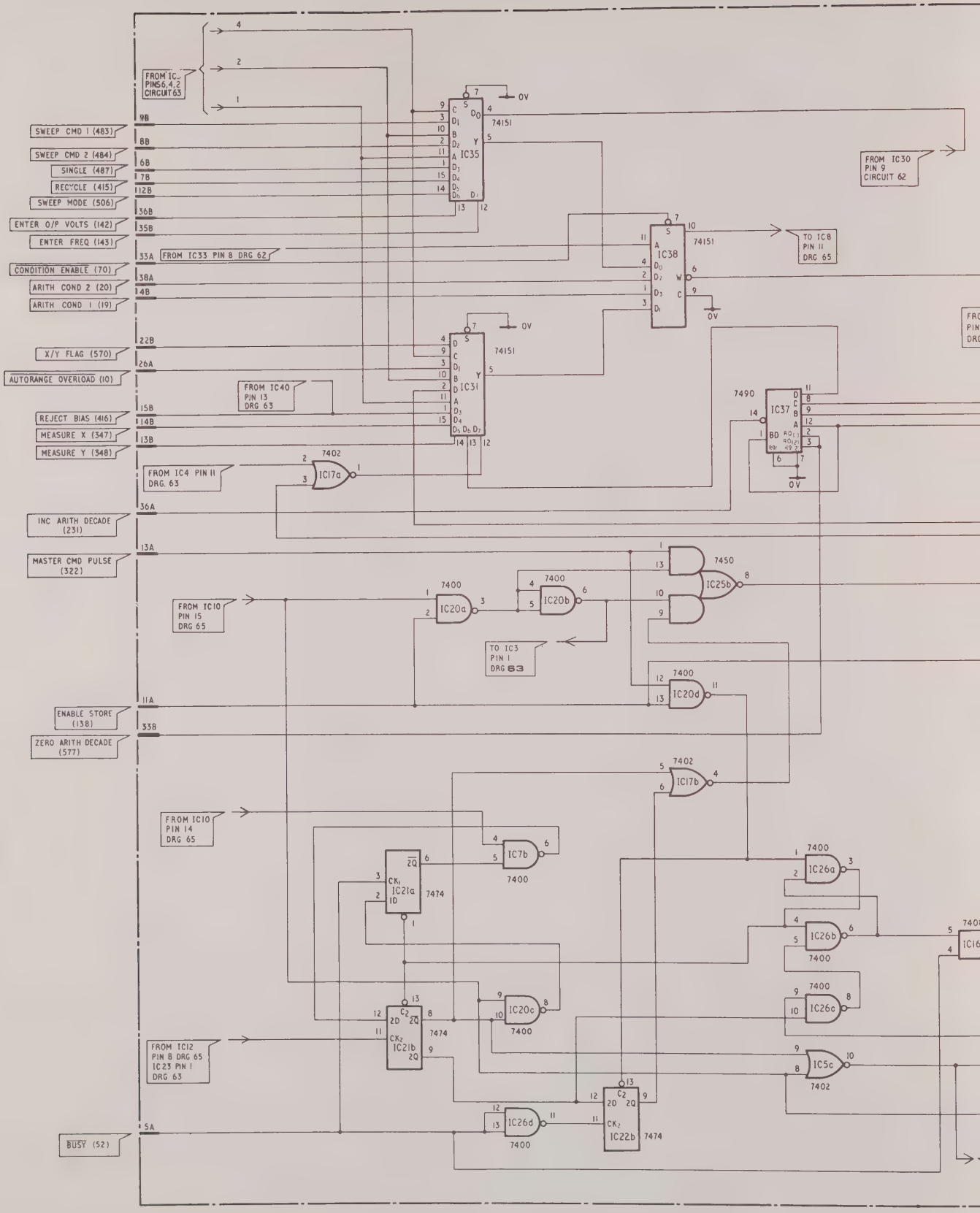
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


RUN BISTABLE
7402
IC30
RUN (438)
X OR Y BISTABLE
7474
IC36
7402
IC29d
X/Y OUTPUT (A) (571)
SWEEP CONDITION
IC30
TO IC35 PIN 4 DRG 64
COMPUTE BISTABLE
7402
IC29a
IC33a
7400
IC34a
IC34b
COMPUTE (69)
TO IC 40 PIN 1
MEASURE BIAS BISTABLE
IC29b
IC36
MEASURE BIAS (323)
TO IC25 PINS 2,3 DRG 63
TO IC40 PIN 9 DRG 63
ONE BIT MEMORY
IC22
TO IC12 PIN 1 DRG.64
7404
IC23e
IC23f
IC23d
IC34f
IC18b
IC16a
IC18a
IC18d
IC18c
SET SWEEP OFF (486)
RESET OVERLOAD (424)
RESET RANGE (427)
INC RANGE (232)
CHANGE FREQ (68)
COMMAND DELAY (81)
IC 38 PIN 11 DRG.64

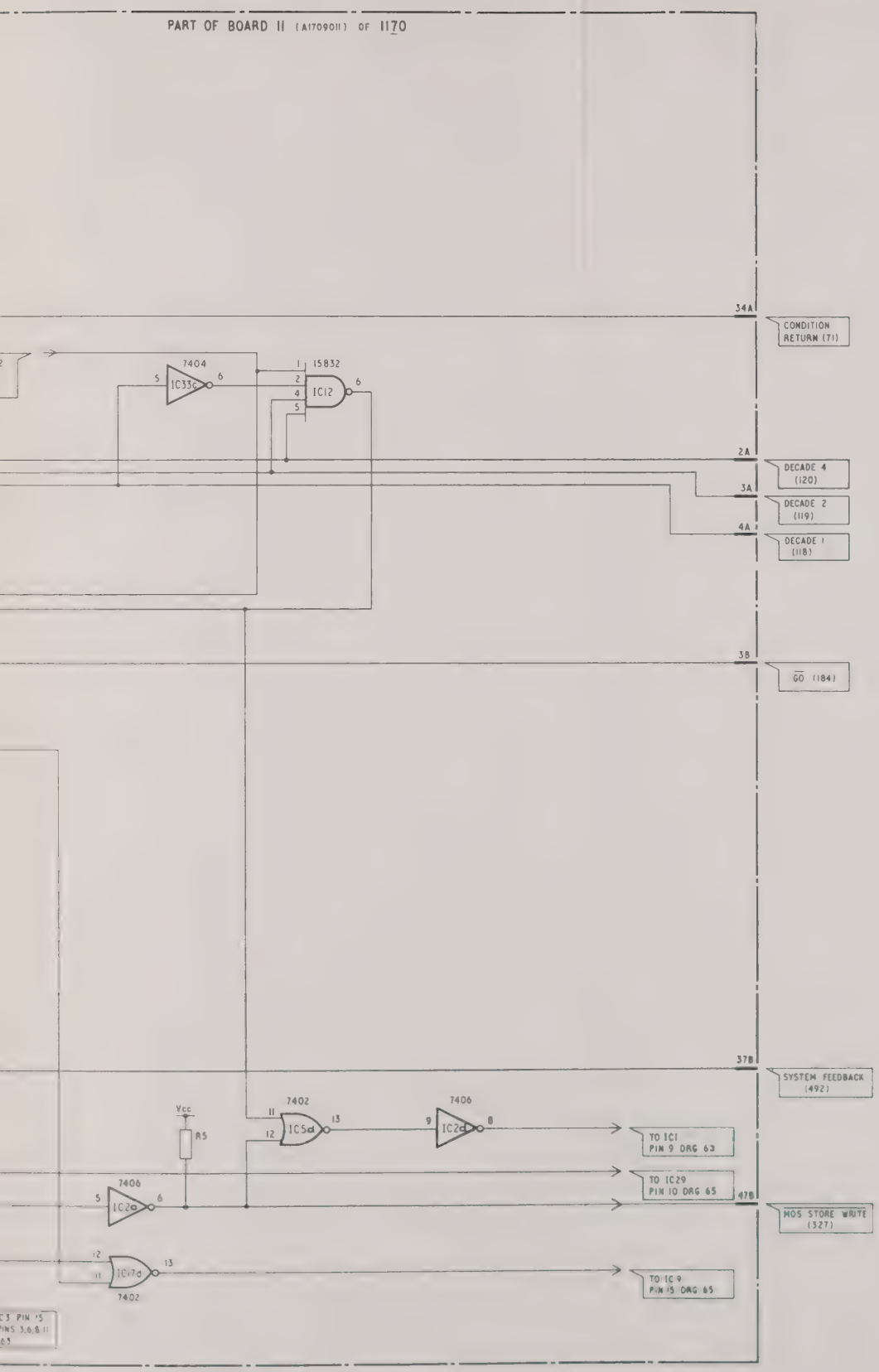


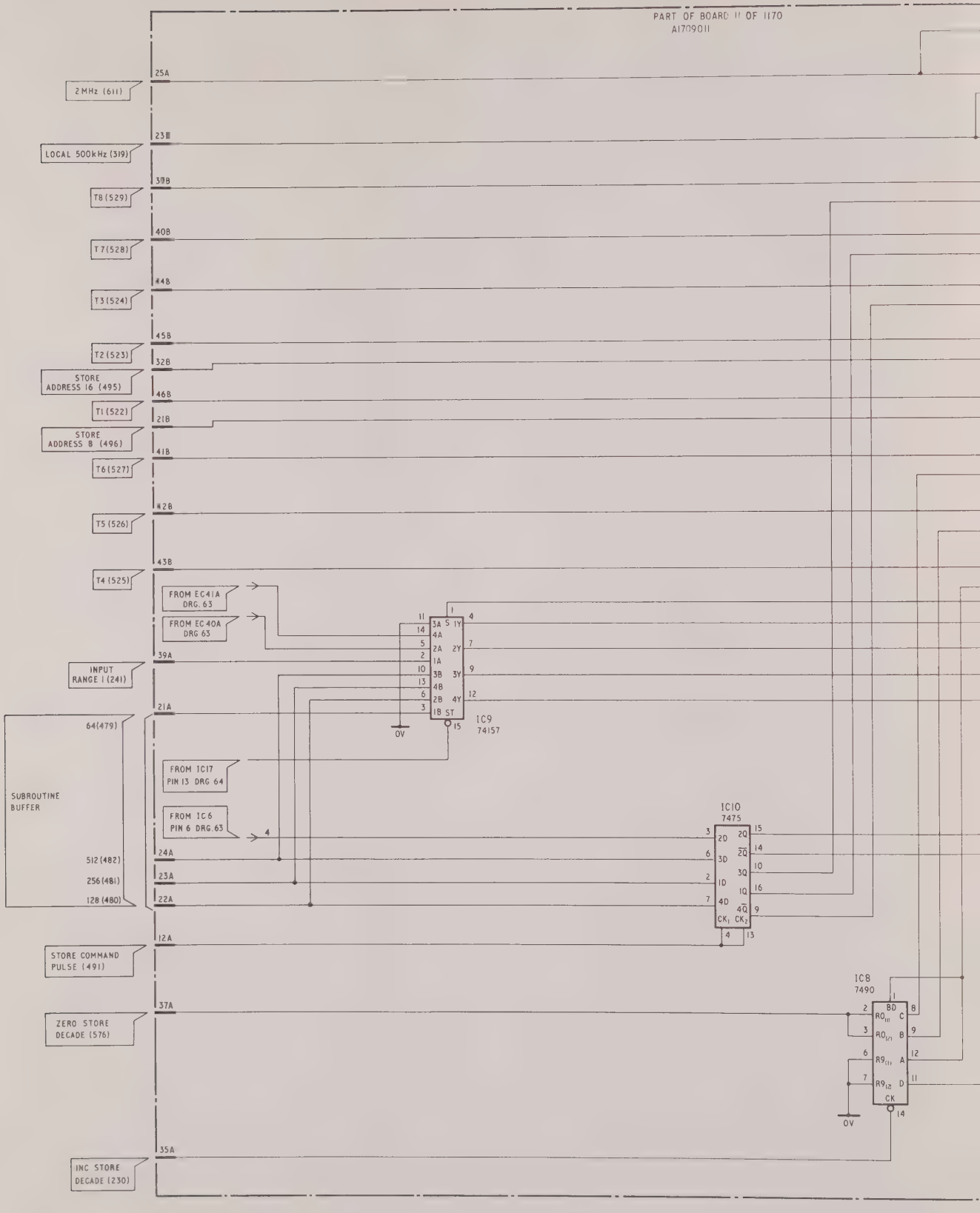
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


IC7c
IC7d
IC25a
R4
R3
R2
R1
52B
BIAS RANGE A (50)
51A
BIAS RANGE B (51)
FROM IC20 PIN 6 DRG 64
51B
MOS STORE DATA INPUT 1 (343)
50B
INPUT 2 (344)
49B
INPUT 4 (345)
48B
INPUT 8 (346)
56A
LOCAL DATA BUS 1 (304)
55A
BUS 2 (305)
54A
BUS 4 (306)
53A
BUS 8 (307)
+5V
R11 R10 R9 R8 R7 R6
470
IC32
INTEL 1301
-9V
IC6
IC5
IC27 PIN 15 CCT 62
IC35 PIN 11 CCT 64
43A
IC27 PIN 14 CCT 62
IC35 PIN 10 CCT 64
44A
IC27 PIN 13 CCT 62
IC35 PIN 9 CCT 64
45A
IC33 PIN 9 CCT 62
46A
47A
48A
49A
50A
ROM OUTPUT 1 (402)
OUTPUT 2 (403)
OUTPUT 4 (404)
OUTPUT 8 (405)
OUTPUT 16 (406)
OUTPUT 32 (407)
OUTPUT 64 (408)
OUTPUT 128 (409)

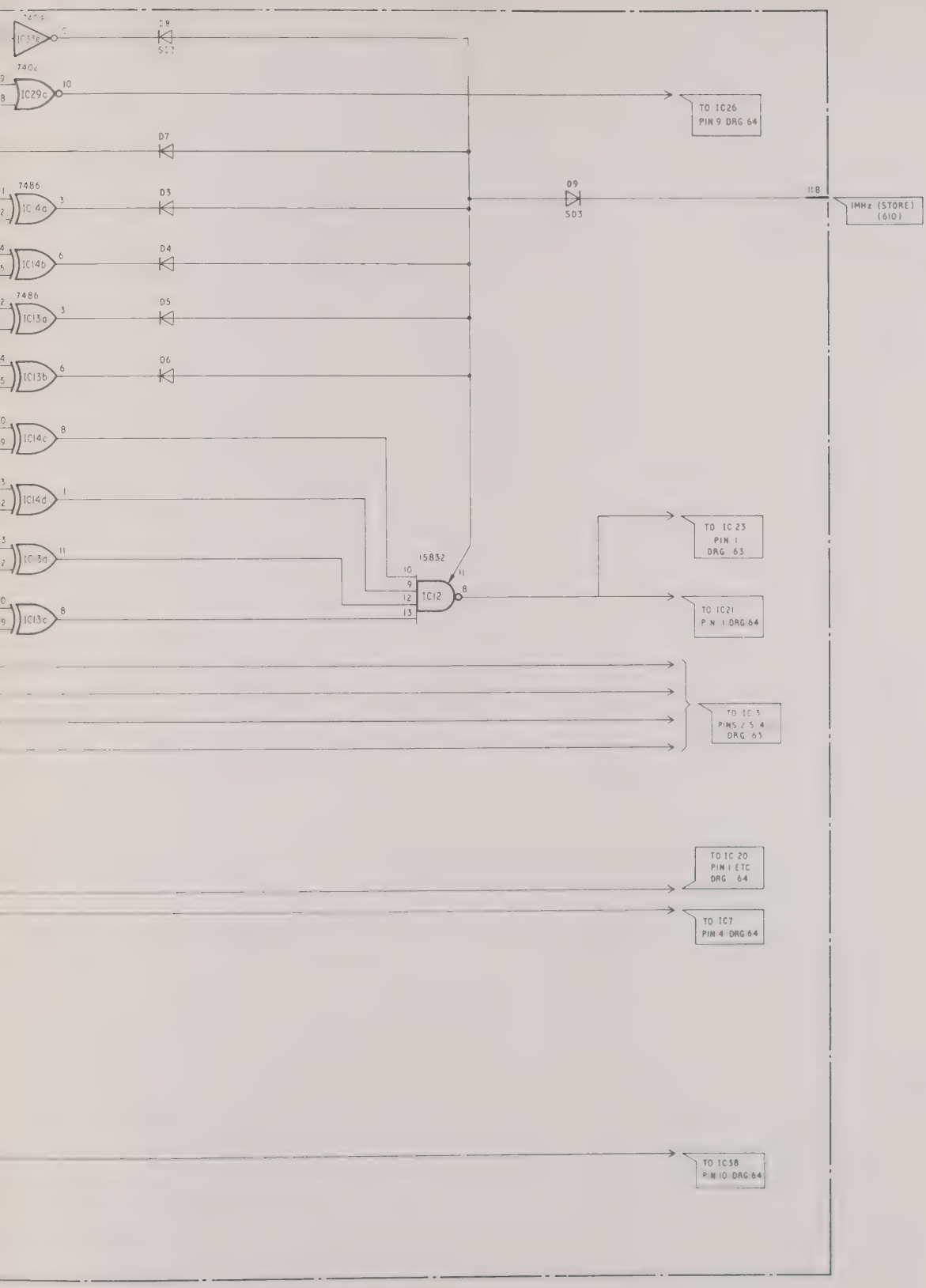


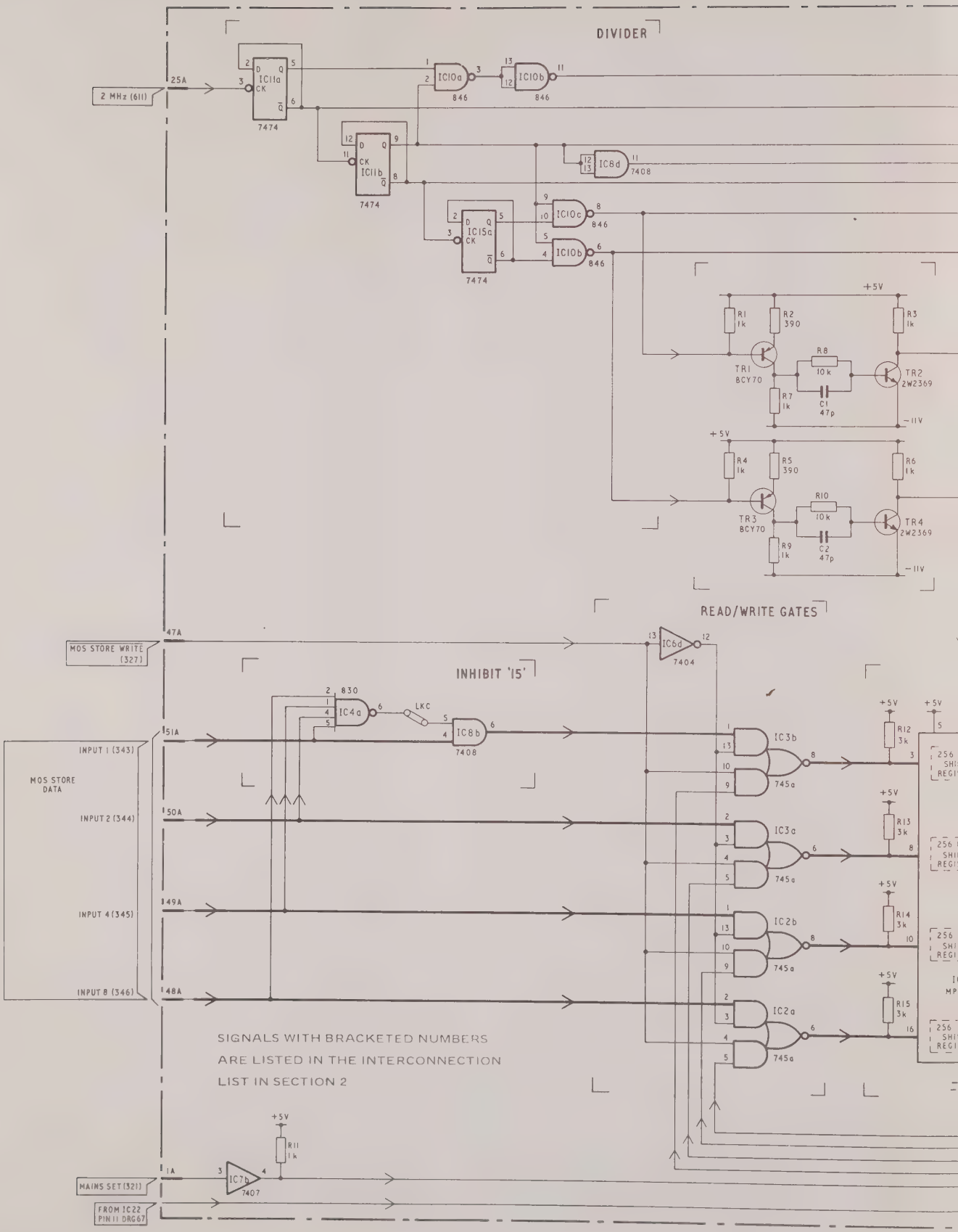
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

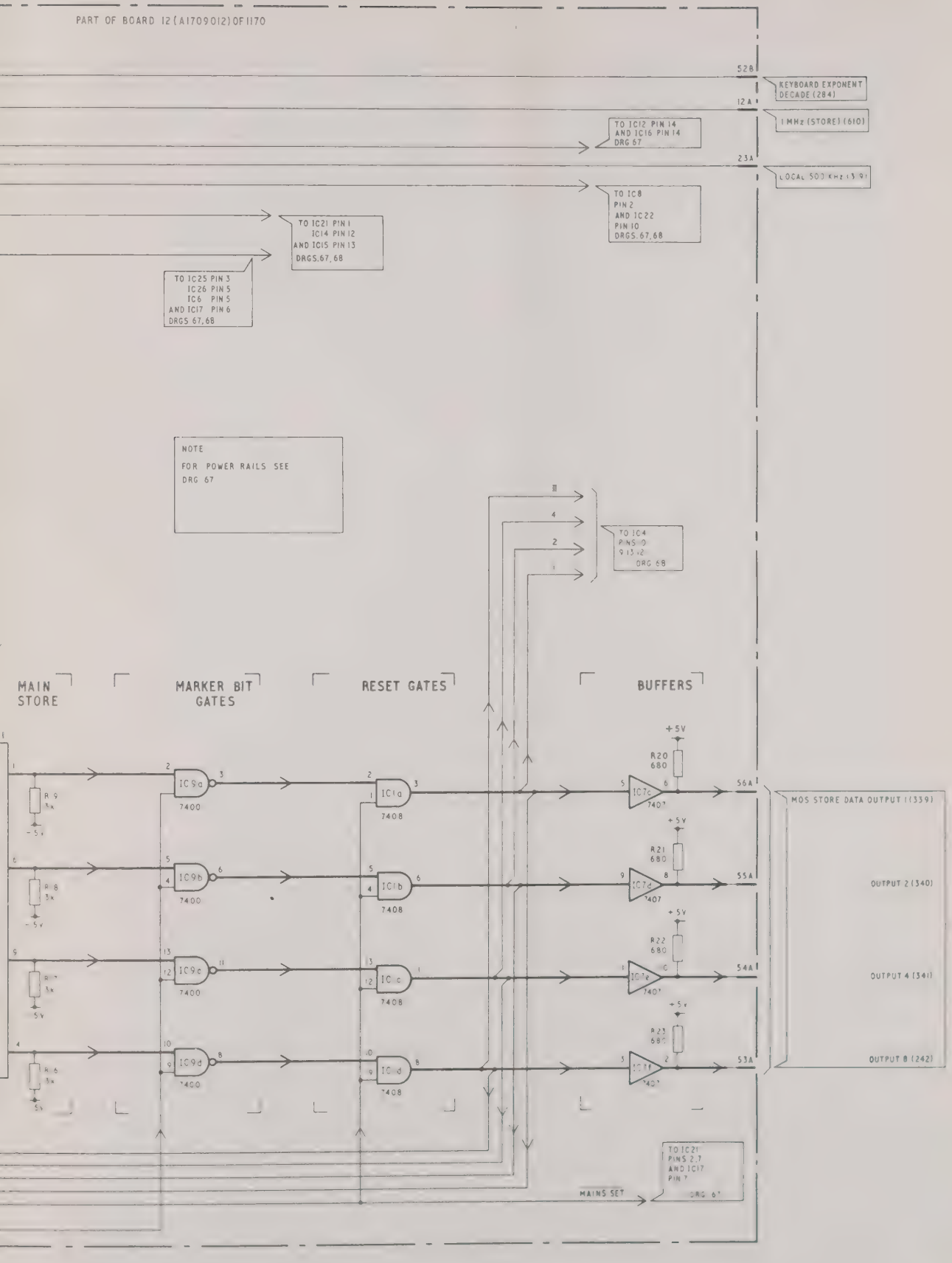

PART OF BOARD II (A1709011) OF 1170
34A
CONDITION RETURN (71)
7404
IC33c
15832
IC12
2A
DECADE 4 (120)
3A
DECADE 2 (119)
4A
DECADE 1 (118)
3B
GO (1184)
37B
SYSTEM FEEDBACK (492)
7402
IC5d
7406
IC2d
Vcc
R5
TO IC1 PIN 9 DRG 63
TO IC29 PIN 10 DRG 65
47B
MOS STORE WRITE (327)
7406
IC2a
IC17a
7402
TO IC9 PIN 15 DRG 65

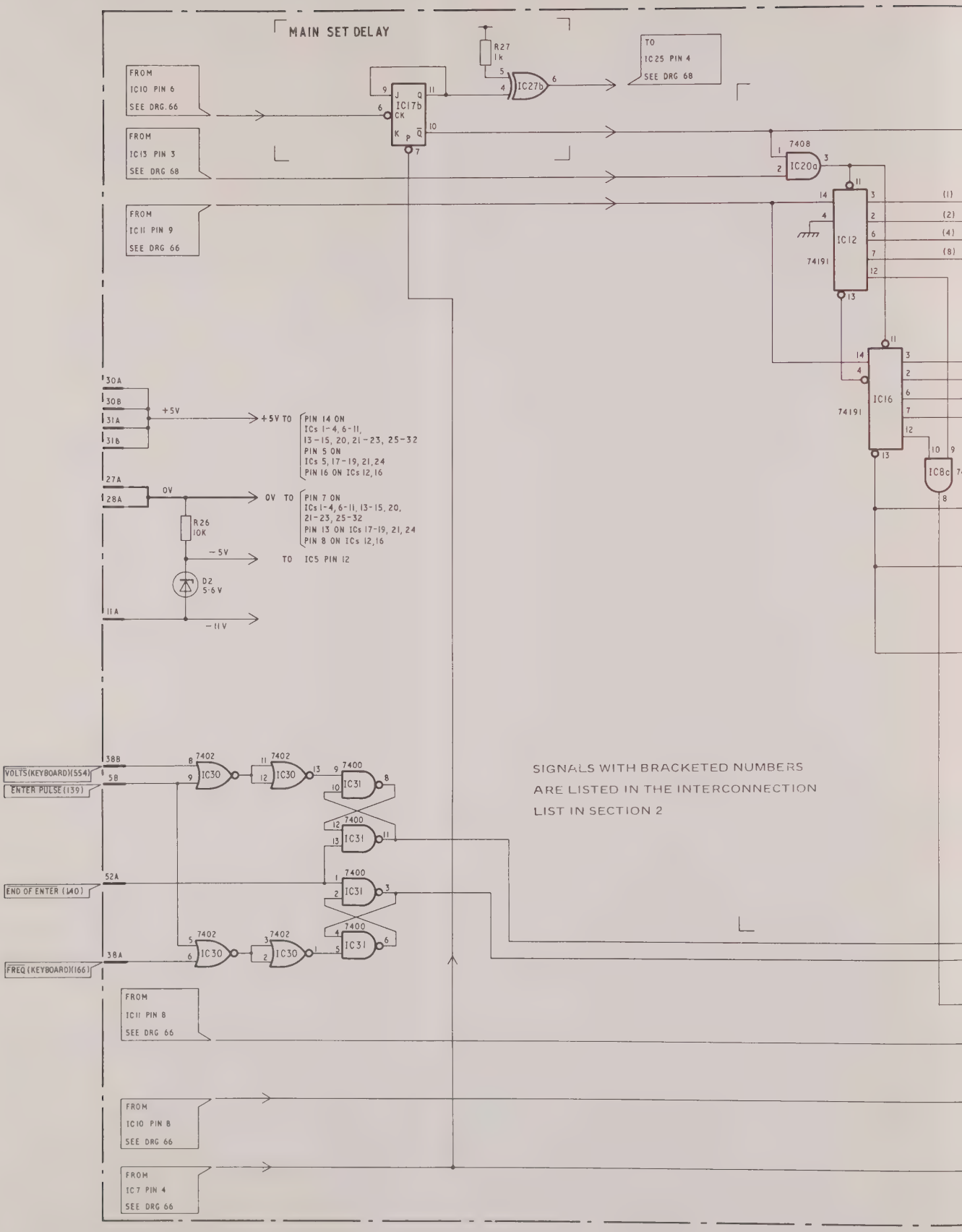


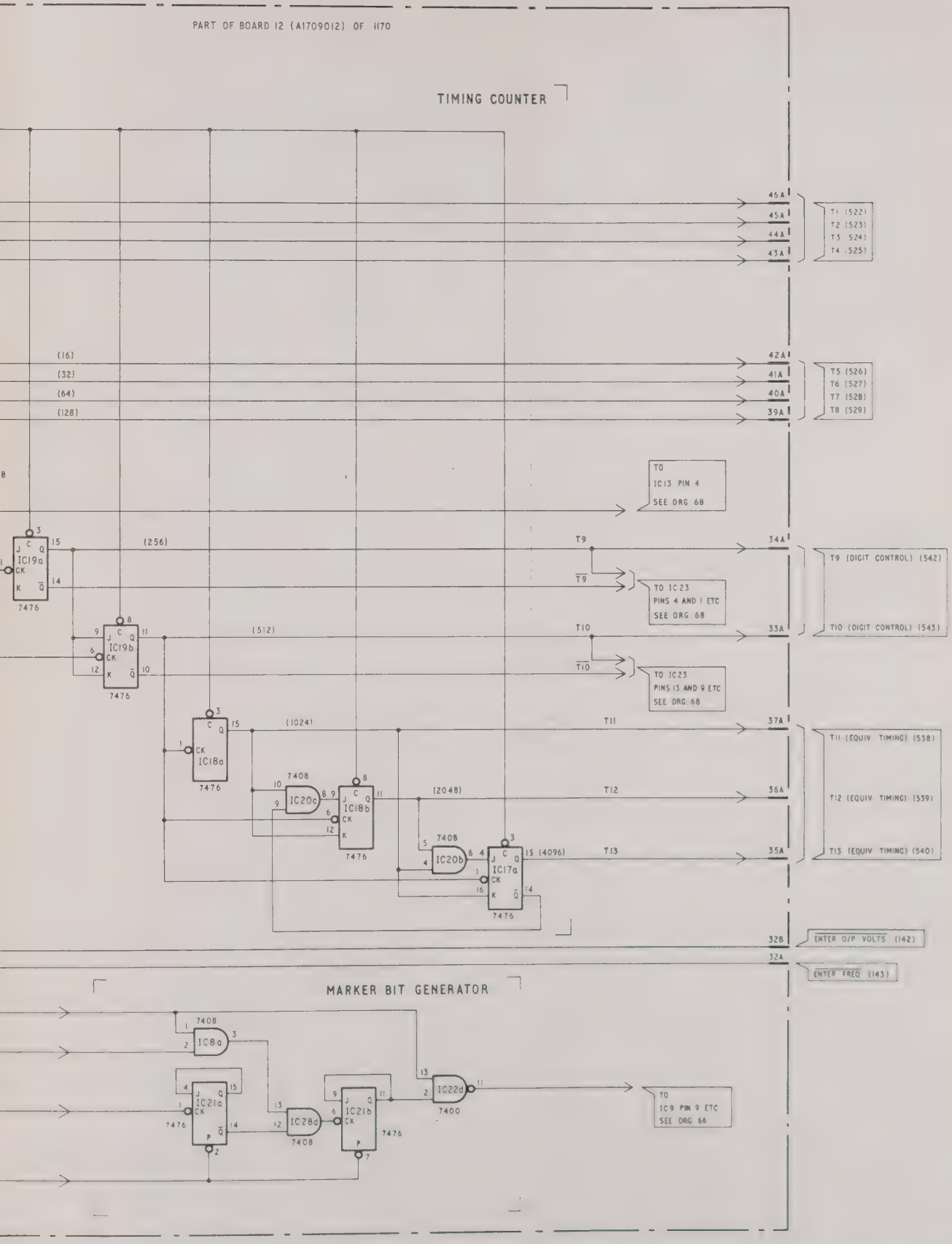
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


IC37e
D8
SD3
7404
IC29c
10
TO IC26
PIN 9 DRG 64
D7
7486
IC 4a
D3
D9
SD3
11B
1MHz (STORE)
(610)
IC14b
D4
7486
IC13a
D5
IC13b
D6
IC14c
IC14d
IC 3a
IC13c
15832
IC12
TO IC 23
PIN 1
DRG 63
TO IC21
P N 1 DRG 64
TO IC 3
PINS 2 5 4
DRG 63
TO IC 20
PIN 1 ETC
DRG 64
TO IC7
PIN 4 DRG 64
TO IC38
PIN 10 DRG 64


DIVIDER
2 MHz (611)
25A
IC11a
7474
IC10a
846
IC10b
846
IC11b
7474
IC8d
7408
IC15a
7474
IC10c
846
IC10b
846
+5V
R1 1k
R2 390
R3 1k
TR1 BCY70
R8 10k
TR2 2W2369
R7 1k
C1 47p
-11V
R4 1k
R5 390
R6 1k
TR3 BCY70
R10 10k
TR4 2W2369
R9 1k
C2 47p
READ/WRITE GATES
MOS STORE WRITE (327)
47A
IC6d
7404
INHIBIT '15'
IC4a
830
LKC
IC8b
7408
51A
INPUT 1 (343)
MOS STORE DATA
INPUT 2 (344)
50A
INPUT 4 (345)
49A
INPUT 8 (346)
48A
IC3b
745a
IC3a
745a
IC2b
745a
IC2a
745a
R12 3k
R13 3k
R14 3k
R15 3k
SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2
R11 1k
IC7b
7407
1A
MAINS SET (321)
FROM IC22 PIN 11 DRG67

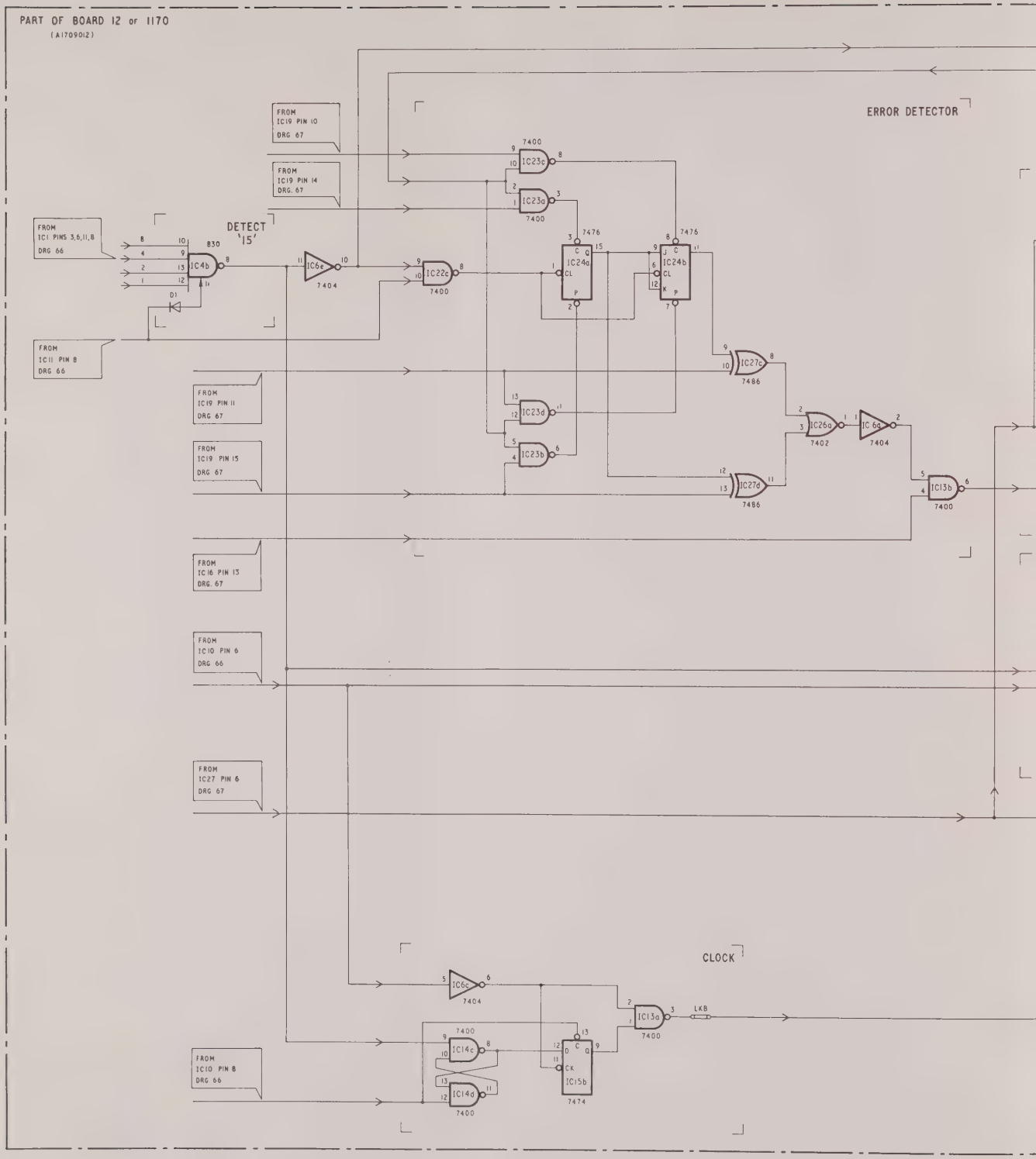

PART OF BOARD 12 (A1709012) OF 1170
528
KEYBOARD EXPONENT DECADE (284)
12A
1 MHz (STORE) (610)
TO IC12 PIN 14 AND IC16 PIN 14 DRG 67
23A
LOCAL 500 KHz (591)
TO IC8 PIN 2 AND IC22 PIN 10 DRGS. 67, 68
TO IC21 PIN 1 IC14 PIN 12 AND IC15 PIN 13 DRGS. 67, 68
TO IC25 PIN 3 IC26 PIN 5 IC6 PIN 5 AND IC17 PIN 6 DRGS 67, 68
NOTE
FOR POWER RAILS SEE DRG 67
TO IC4 PINS 10 9 13 12 DRG 68
MAIN STORE
MARKER BIT GATES
RESET GATES
BUFFERS
+5V
R20 680
R21 680
R22 680
R23 680
IC9a
IC9b
IC9c
IC9d
7400
IC1a
IC1b
IC1c
IC1d
7408
IC7c
IC7d
7407
56A
55A
54A
53A
MOS STORE DATA OUTPUT 1 (339)
OUTPUT 2 (340)
OUTPUT 4 (341)
OUTPUT 8 (242)
TO IC21 PINS 2, 7 AND IC17 PIN 7
MAINS SET
DRG 67


MAIN SET DELAY
FROM IC10 PIN 6 SEE DRG. 66
FROM IC13 PIN 3 SEE DRG 68
FROM IC11 PIN 9 SEE DRG 66
IC17b
R27 1k
IC27b
TO IC25 PIN 4 SEE DRG 68
7408
IC20a
IC12
74191
IC16
IC8c
30A
30B
31A
31B
+5V
+5V TO
PIN 14 ON ICs 1-4, 6-11, 13-15, 20, 21-23, 25-32
PIN 5 ON ICs 5, 17-19, 21, 24
PIN 16 ON ICs 12, 16
27A
28A
0V
0V TO
PIN 7 ON ICs 1-4, 6-11, 13-15, 20, 21-23, 25-32
PIN 13 ON ICs 17-19, 21, 24
PIN 8 ON ICs 12, 16
R26 10K
-5V
TO IC5 PIN 12
D2 5·6 V
11A
-11V
38B
VOLTS (KEYBOARD) (554)
5B
ENTER PULSE (139)
52A
END OF ENTER (140)
38A
FREQ (KEYBOARD) (166)
7402
IC30
7400
IC31
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2
FROM IC11 PIN 8 SEE DRG 66
FROM IC10 PIN 8 SEE DRG 66
FROM IC7 PIN 4 SEE DRG 66

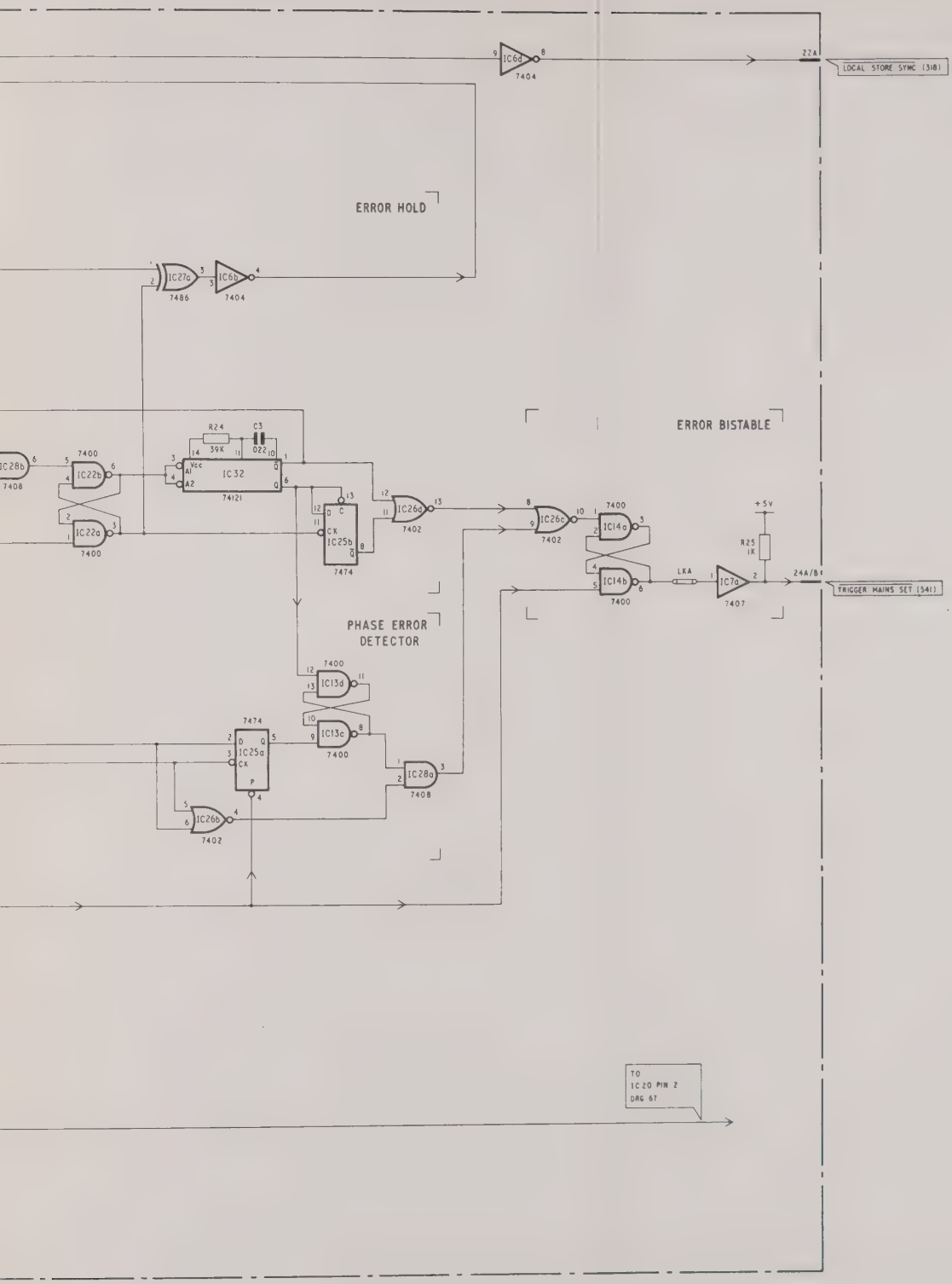


TIMING COUNTER & MARKER BIT GENERATOR

D11707067-02

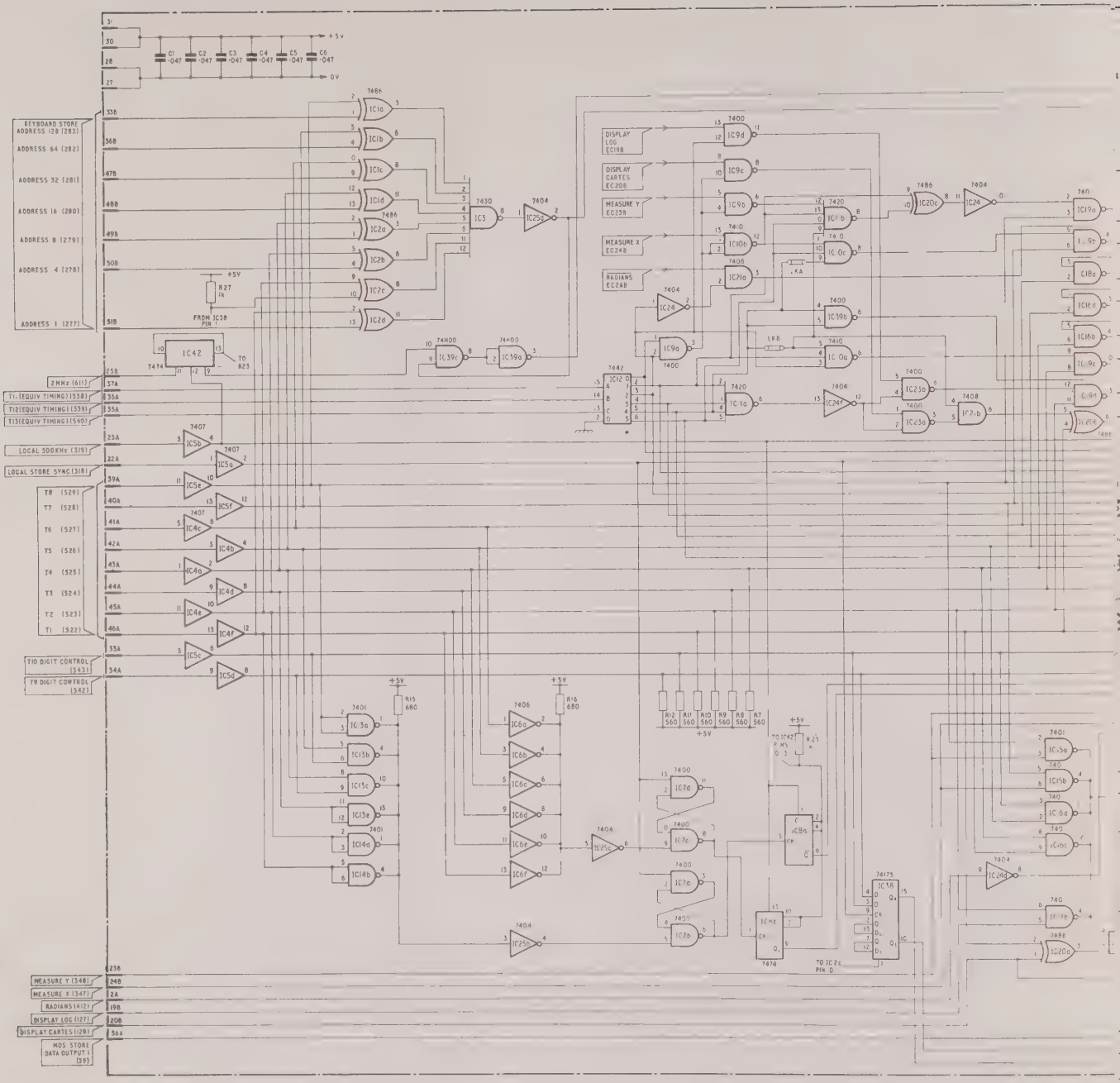


SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2

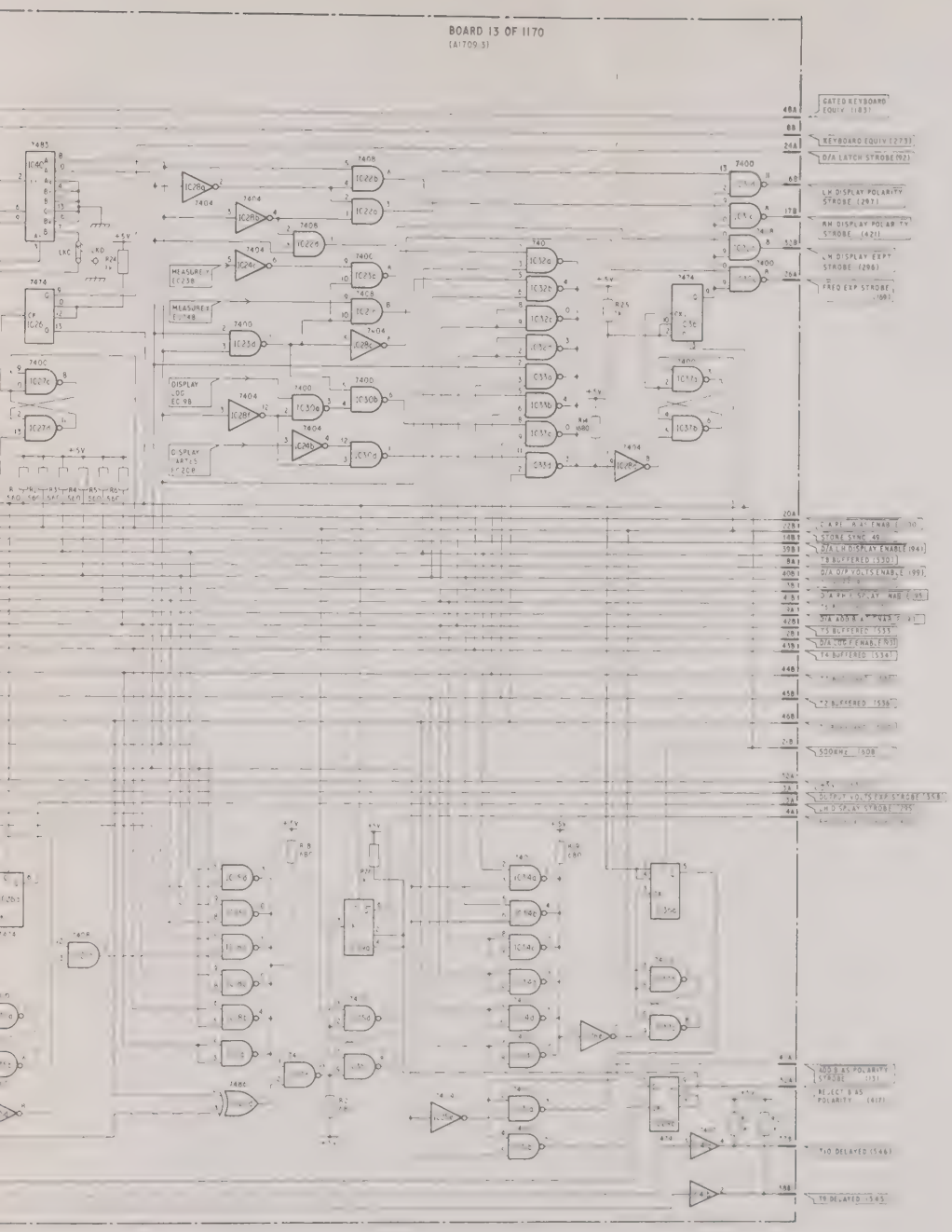


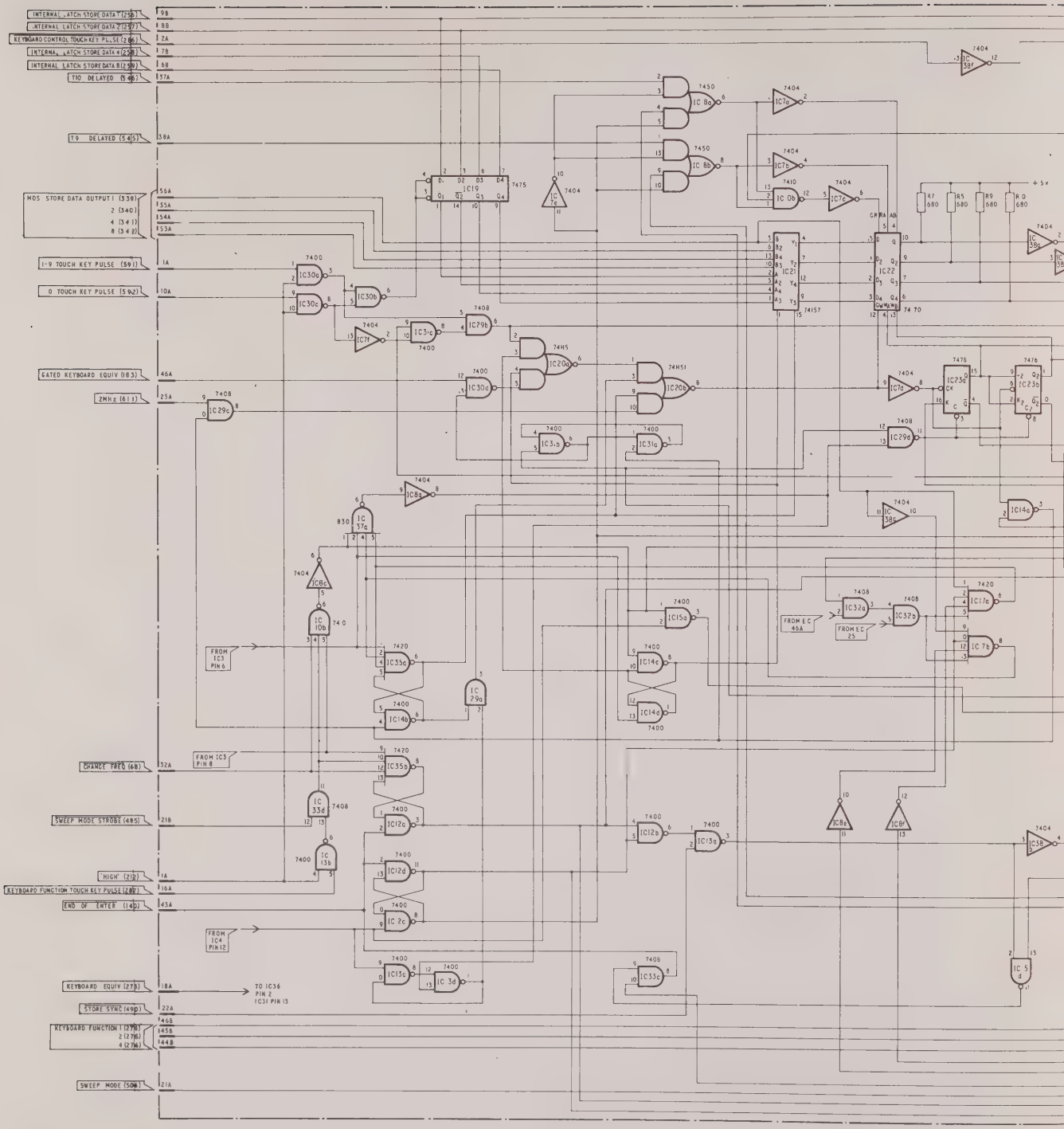
ERROR DETECTION LOGIC
BOARD 12

D11707068 - 02

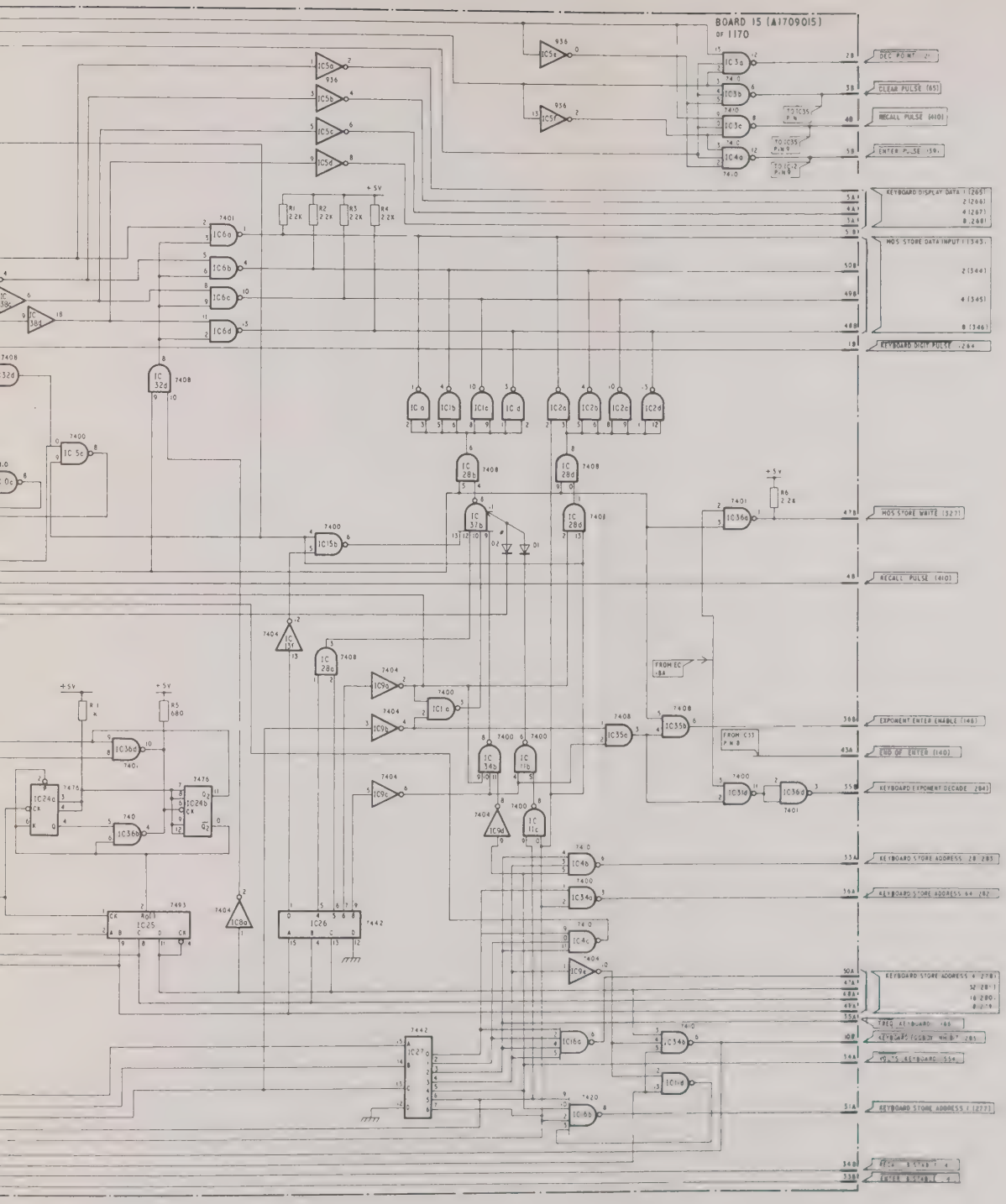


SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2


BOARD 13 OF 1170
(A1709.3)
GATED KEYBOARD (EQUIV 1183)
KEYBOARD EQUIV (273)
D/A LATCH STROBE (92)
LM DISPLAY POLARITY STROBE (297)
RM DISPLAY POLARITY STROBE (421)
LM DISPLAY EXPT STROBE (298)
FREQ EXP STROBE (181)
T5 BUFFERED (533)
T4 BUFFERED (534)
T2 BUFFERED (538)
500KHz (508)
OUTPUT VOLTS EXP STROBE (358)
RM DISPLAY STROBE (295)
T10 DELAYED (546)
T9 DELAYED (545)



SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2


BOARD 15 (A1709015)
OF 1170
DEC POINT
CLEAR PULSE (65)
RECALL PULSE (410)
ENTER PULSE (59)
KEYBOARD DISPLAY DATA
MOS STORE DATA INPUT
KEYBOARD DIGIT PULSE
MOS STORE WRITE (327)
RECALL PULSE (410)
FROM EC
EXPONENT ENTER ENABLE (148)
END OF ENTER (140)
KEYBOARD EXPONENT DECADE
KEYBOARD STORE ADDRESS
KEYBOARD STORE ADDRESS
KEYBOARD STORE ADDRESS
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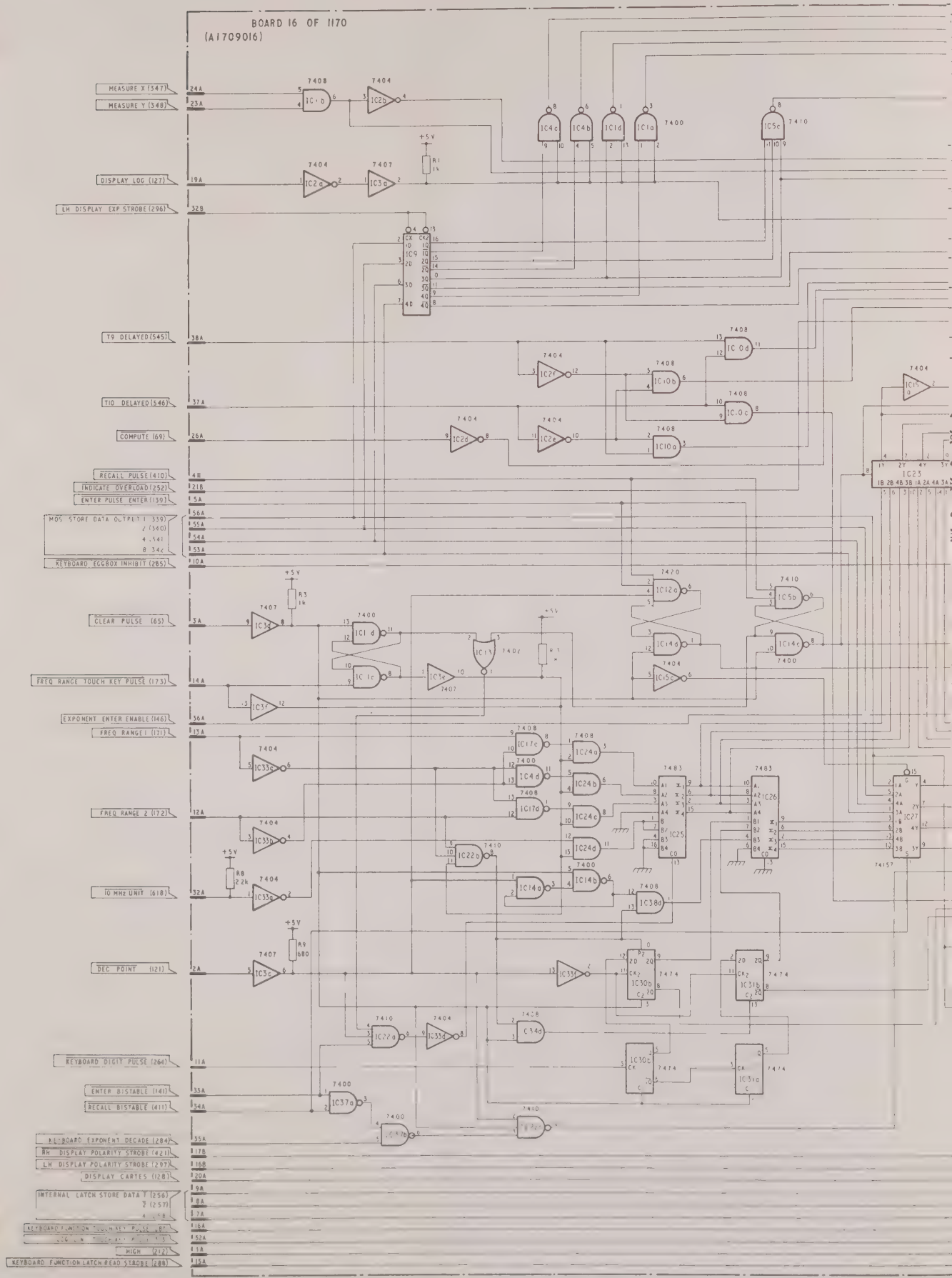
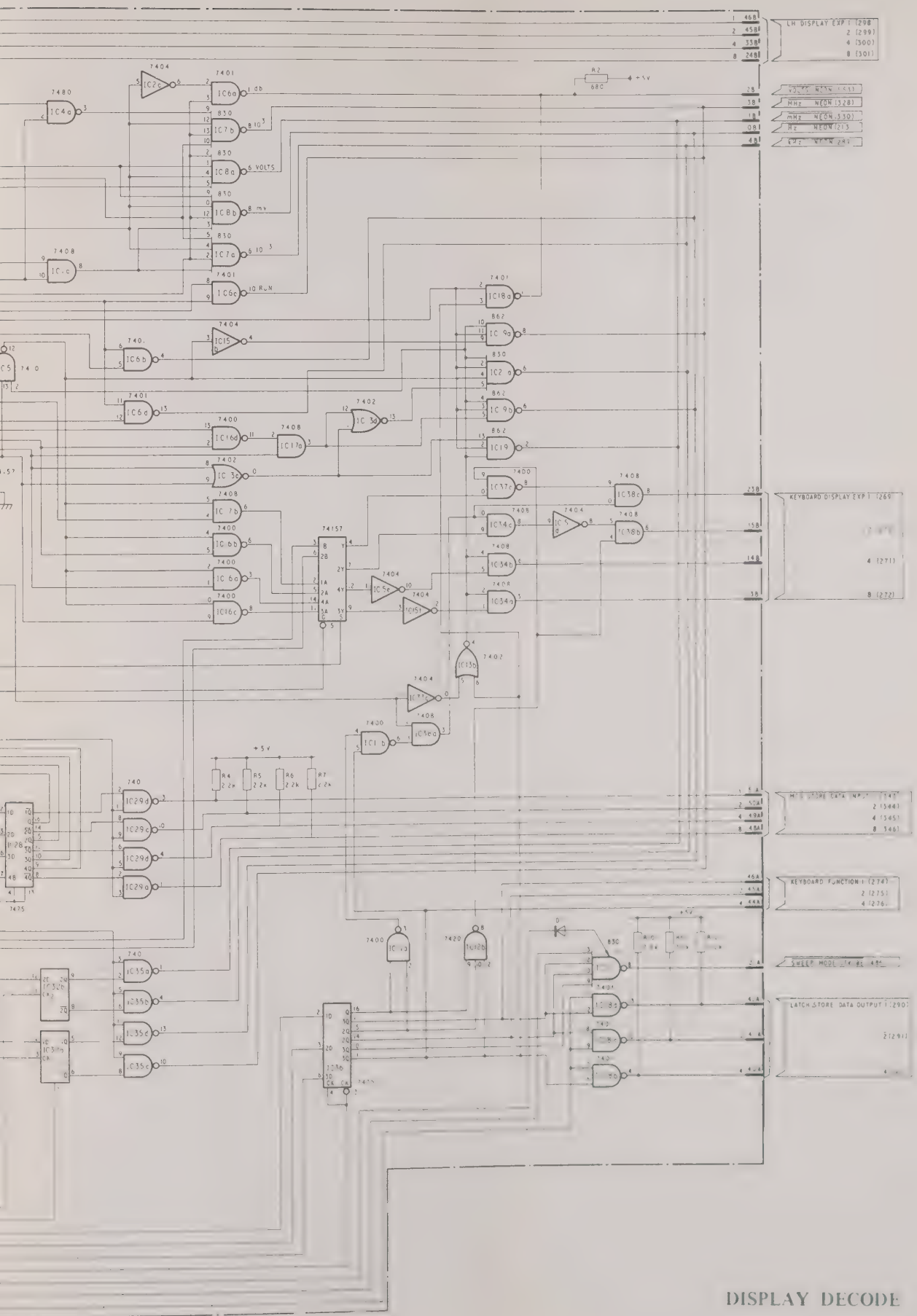
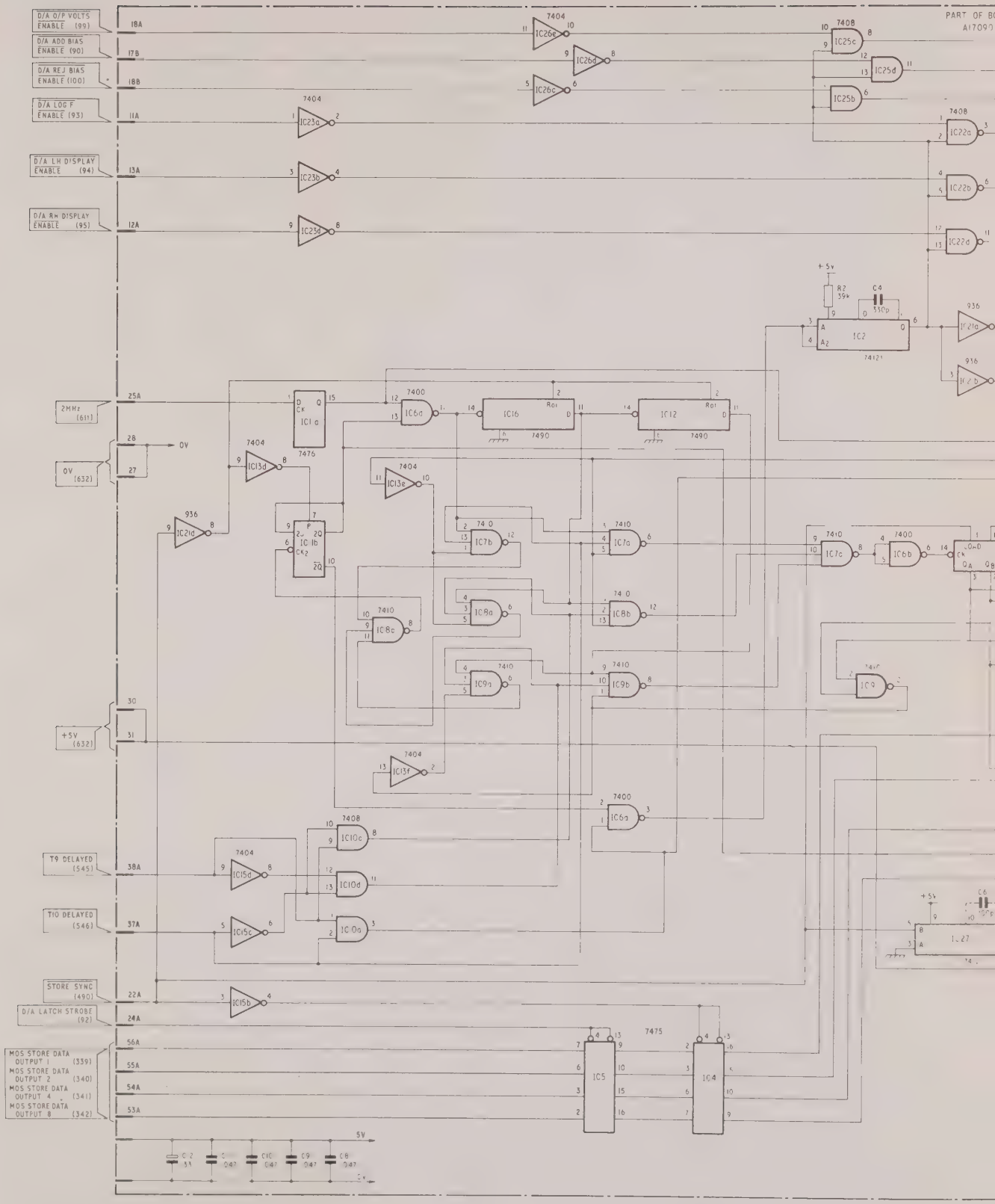
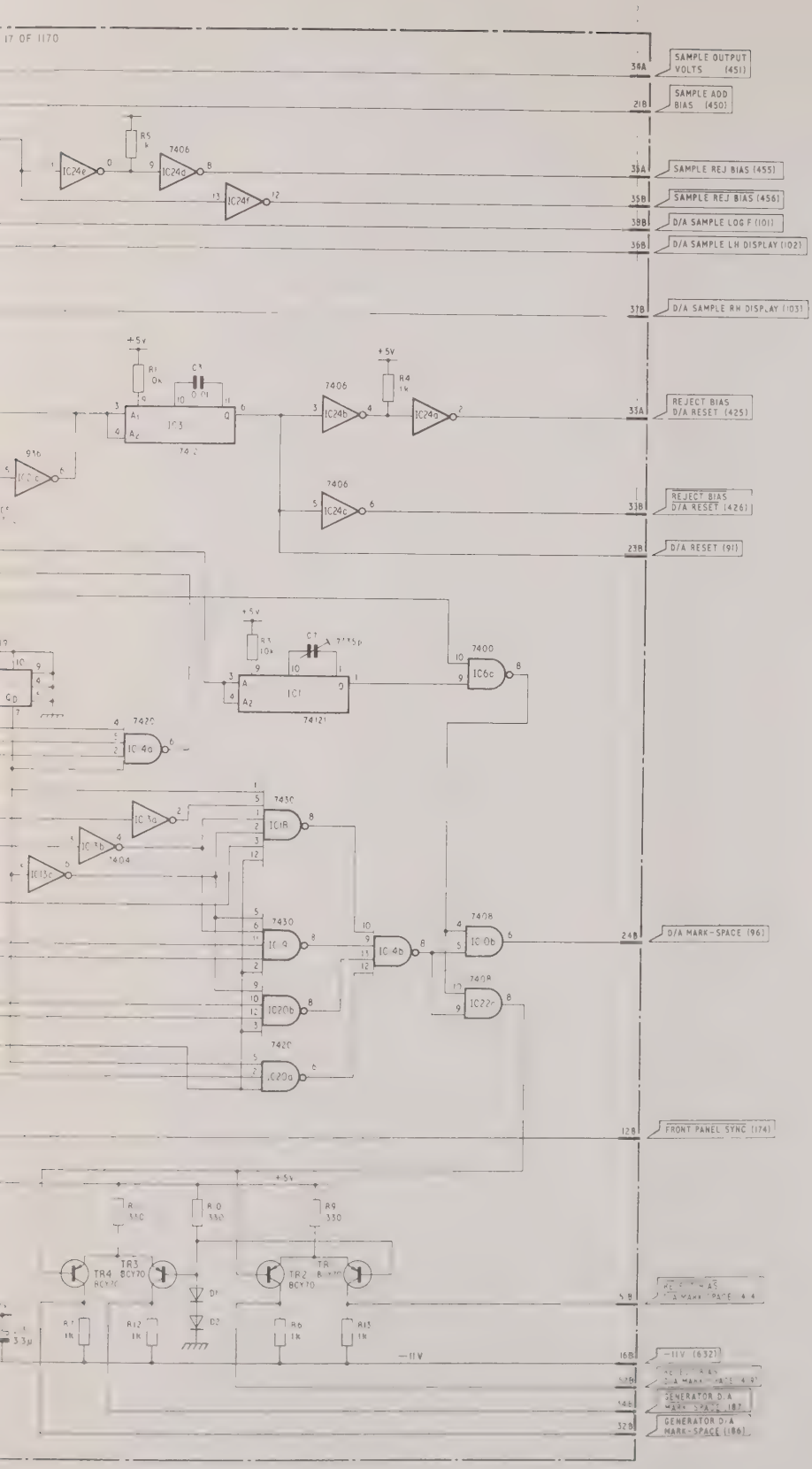
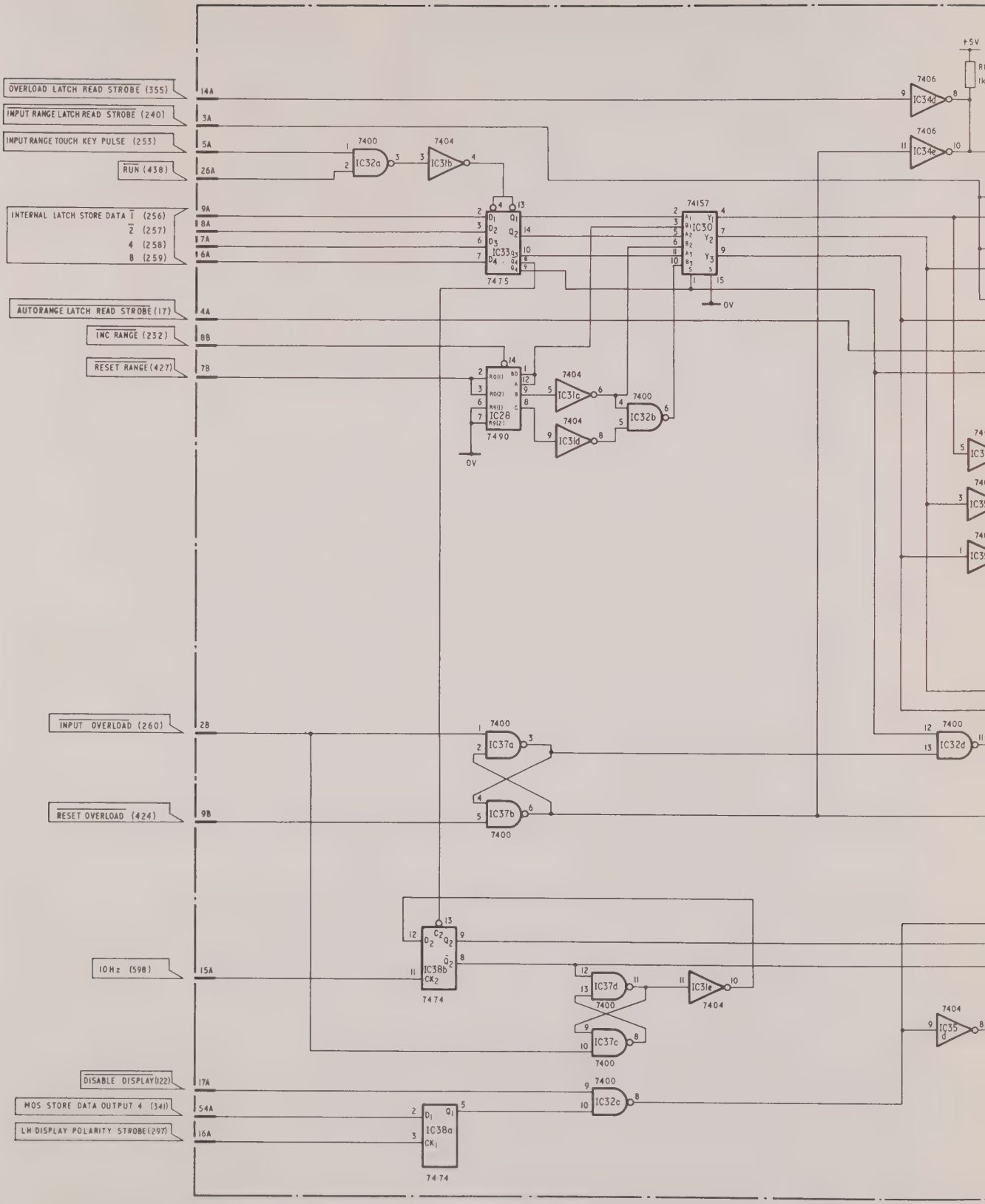

BOARD 16 OF 1170
(A1709016)
MEASURE X (347)
MEASURE Y (348)
DISPLAY LOG (127)
LH DISPLAY EXP STROBE (296)
T9 DELAYED (545)
T10 DELAYED (546)
COMPUTE (69)
RECALL PULSE (410)
INDICATE OVERLOAD (252)
ENTER PULSE ENTER (139)
MOS STORE DATA OUTPUT 1 (339)
2 (340)
4 (341)
8 (342)
KEYBOARD ECGBOX INHIBIT (285)
CLEAR PULSE (65)
FREQ RANGE TOUCH KEY PULSE (173)
EXPONENT ENTER ENABLE (146)
FREQ RANGE 1 (171)
FREQ RANGE 2 (172)
10 MHz UNIT (618)
DEC POINT (121)
KEYBOARD DIGIT PULSE (264)
ENTER BISTABLE (141)
RECALL BISTABLE (411)
KEYBOARD EXPONENT DECADE (284)
RH DISPLAY POLARITY STROBE (421)
LH DISPLAY POLARITY STROBE (297)
DISPLAY CARTES (128)
INTERNAL LATCH STORE DATA 1 (256)
2 (257)
4 (258)
KEYBOARD FUNCTION TOUCH KEY PULSE (87)
KEYBOARD FUNCTION LATCH PULSE (88)
HIGH (212)
KEYBOARD FUNCTION LATCH READ STROBE (288)
+5V
7400
7404
7407
7408
7410
7420
7474
7483
74157


LH DISPLAY EXP I (298
2 (299)
4 (300)
8 (301)
KEYBOARD DISPLAY EXP I (269
4 (271)
8 (272)
KEYBOARD FUNCTION I (274)
2 (275)
4 (276)
LATCH STORE DATA OUTPUT I (290)
74157
74153
74151
74154
74145
74175
74298
74LS138
+5V
6 VOLTS
10 RUN

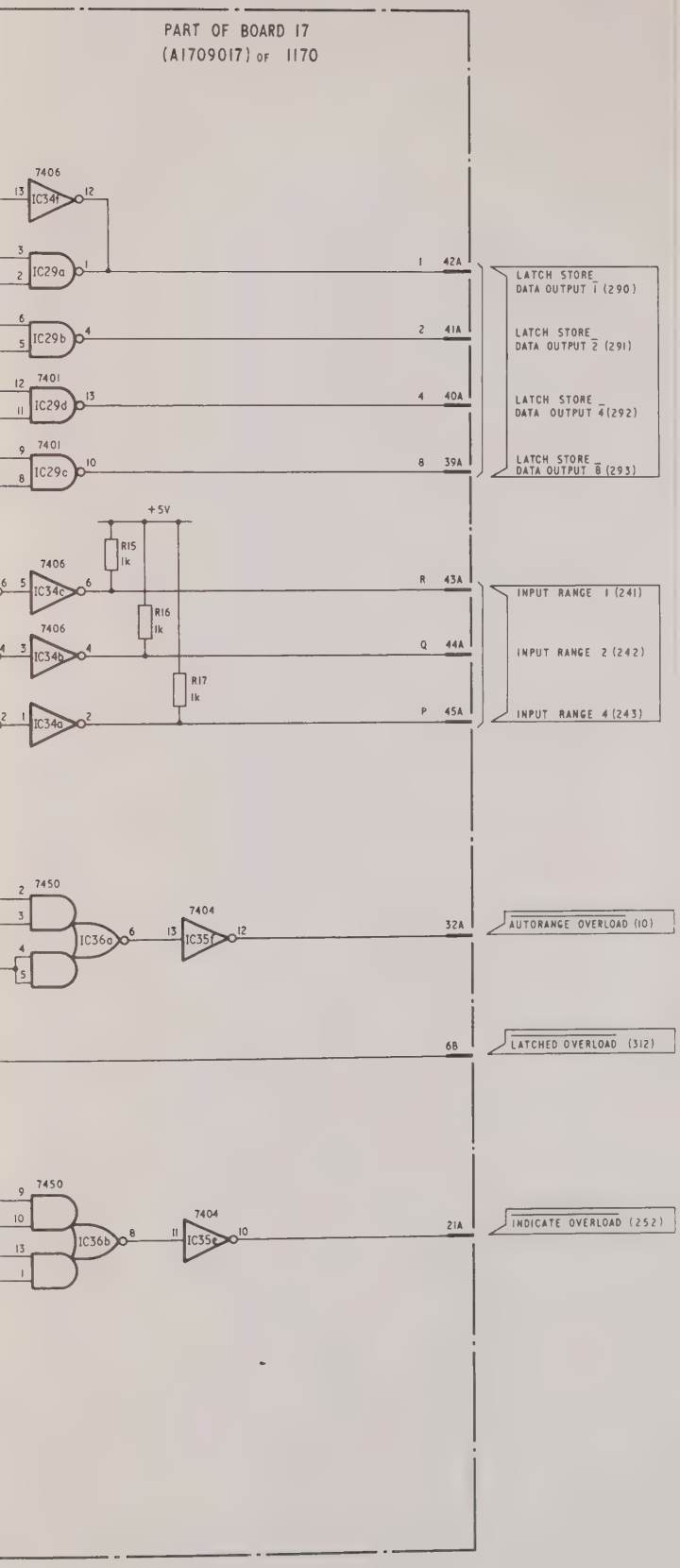


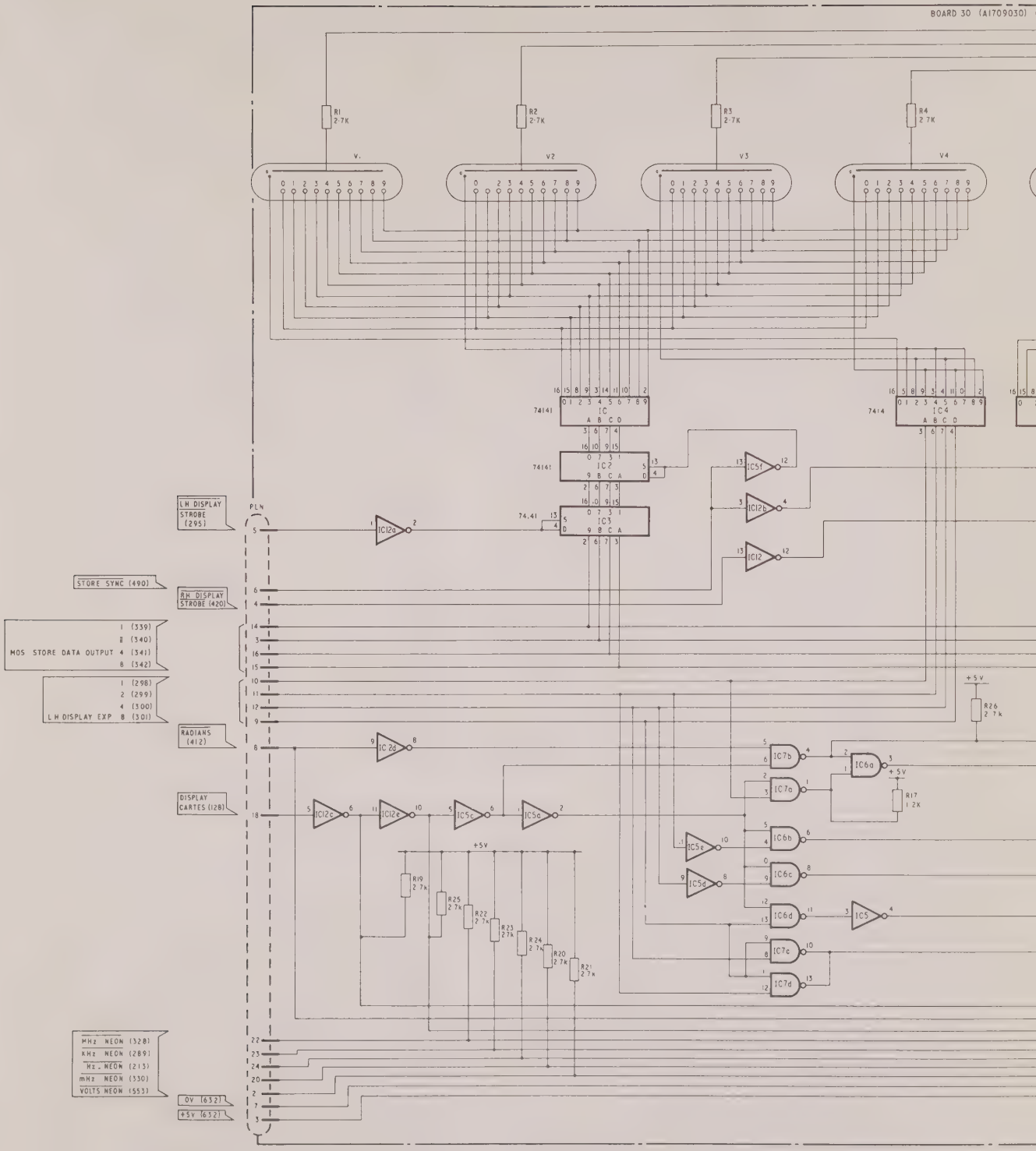
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


17 OF 1170
SAMPLE OUTPUT VOLTS (451)
SAMPLE ADD BIAS (450)
SAMPLE REJ BIAS (455)
SAMPLE REJ BIAS (456)
D/A SAMPLE LOG F (101)
D/A SAMPLE LH DISPLAY (102)
D/A SAMPLE RH DISPLAY (103)
REJECT BIAS D/A RESET (425)
REJECT BIAS D/A RESET (426)
D/A RESET (91)
D/A MARK-SPACE (96)
FRONT PANEL SYNC (174)
-11V (632)
GENERATOR D/A MARK-SPACE (187)
GENERATOR D/A MARK-SPACE (186)
7406
7400
7420
7430
7408
74121
74123
+5V
-11V

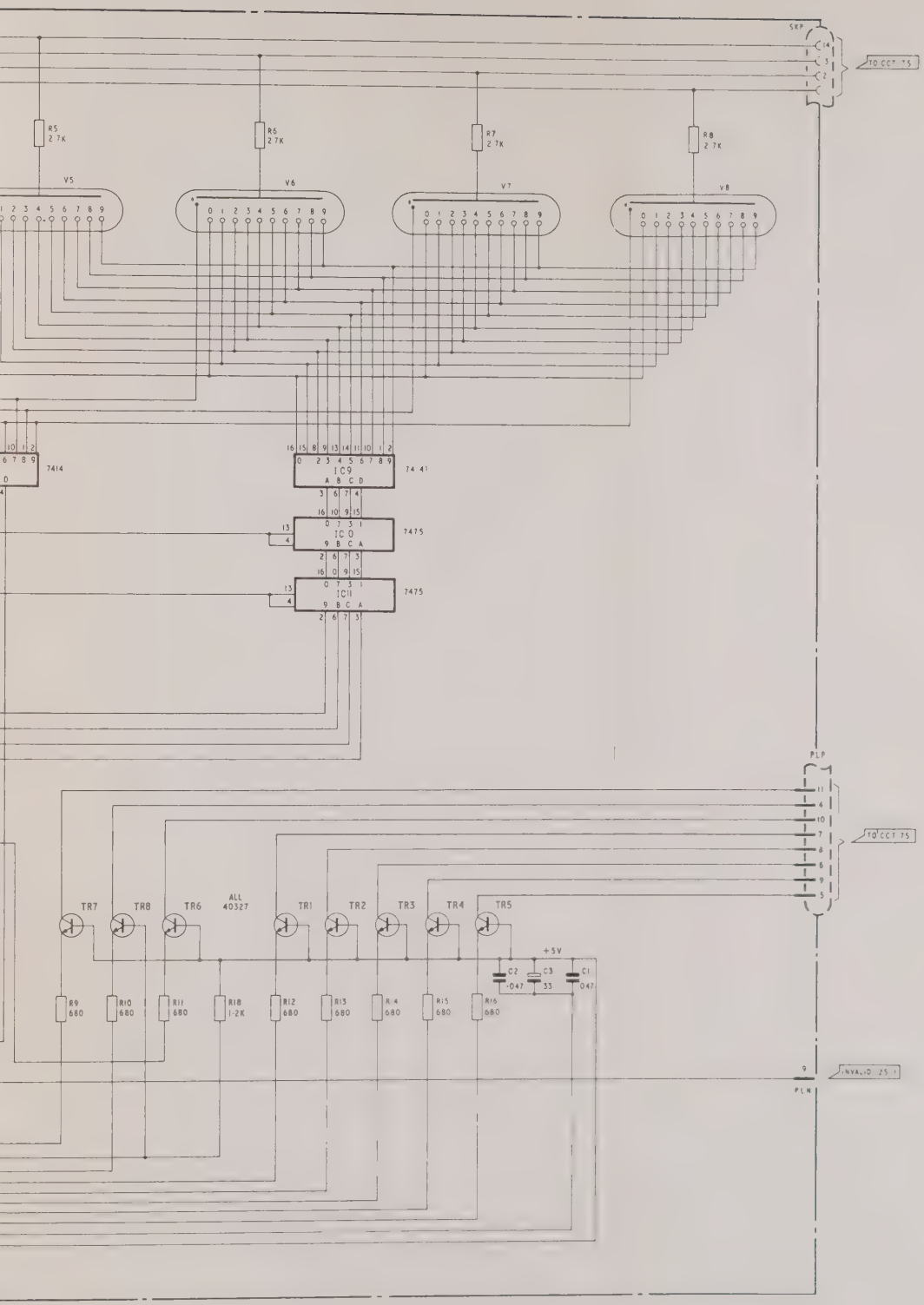


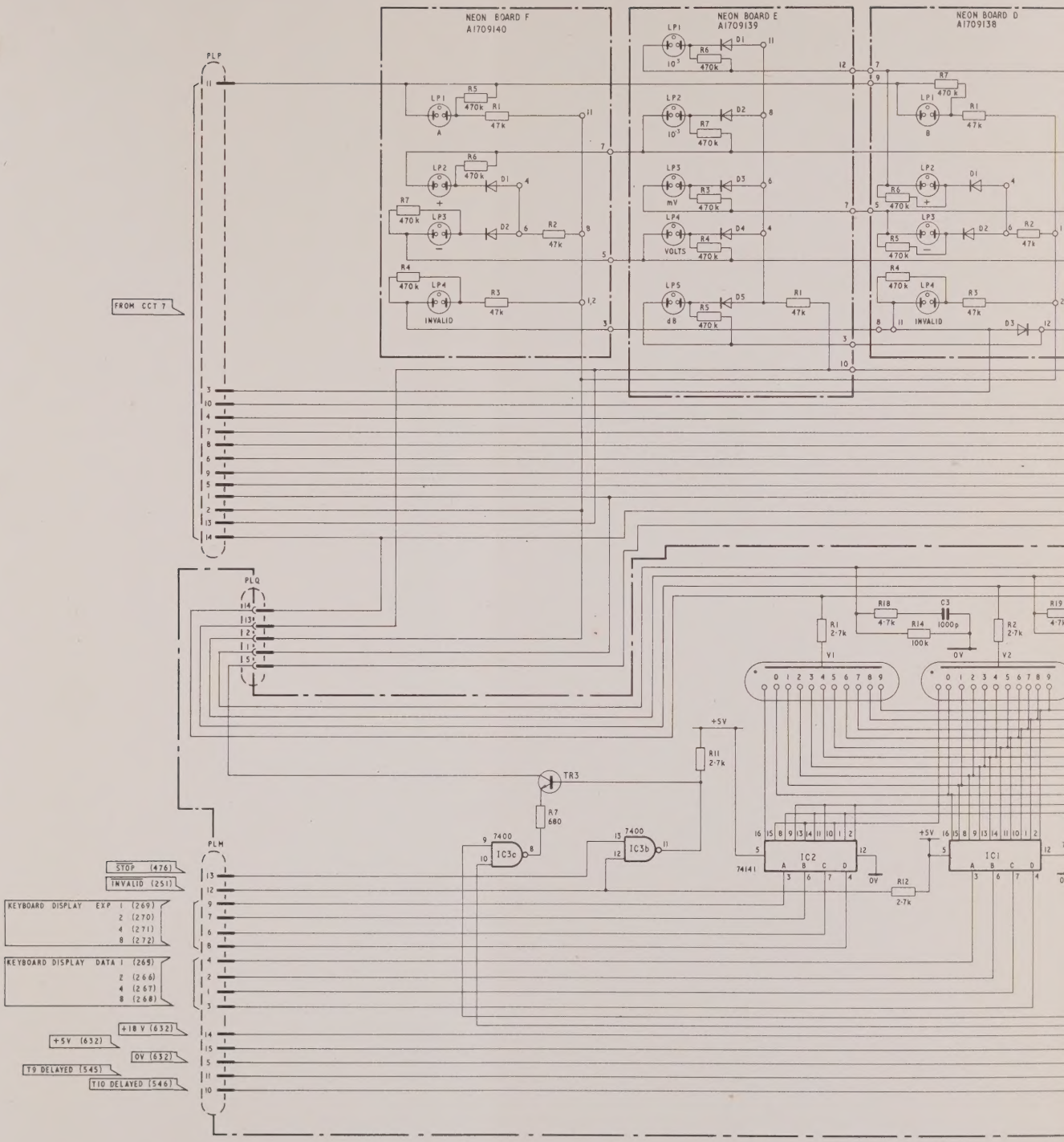
SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2


PART OF BOARD 17
(A1709017) OF 1170
7406
IC34f
IC29a
IC29b
7401
IC29d
7401
IC29c
1 42A
LATCH STORE DATA OUTPUT 1 (290)
2 41A
LATCH STORE DATA OUTPUT 2 (291)
4 40A
LATCH STORE DATA OUTPUT 4 (292)
8 39A
LATCH STORE DATA OUTPUT 8 (293)
+5V
R15 1k
R16 1k
R17 1k
7406
IC34c
7406
IC34b
IC34a
R 43A
INPUT RANGE 1 (241)
Q 44A
INPUT RANGE 2 (242)
P 45A
INPUT RANGE 4 (243)
7450
IC36a
7404
IC35f
32A
AUTORANGE OVERLOAD (10)
6B
LATCHED OVERLOAD (312)
7450
IC36b
7404
IC35e
21A
INDICATE OVERLOAD (252)

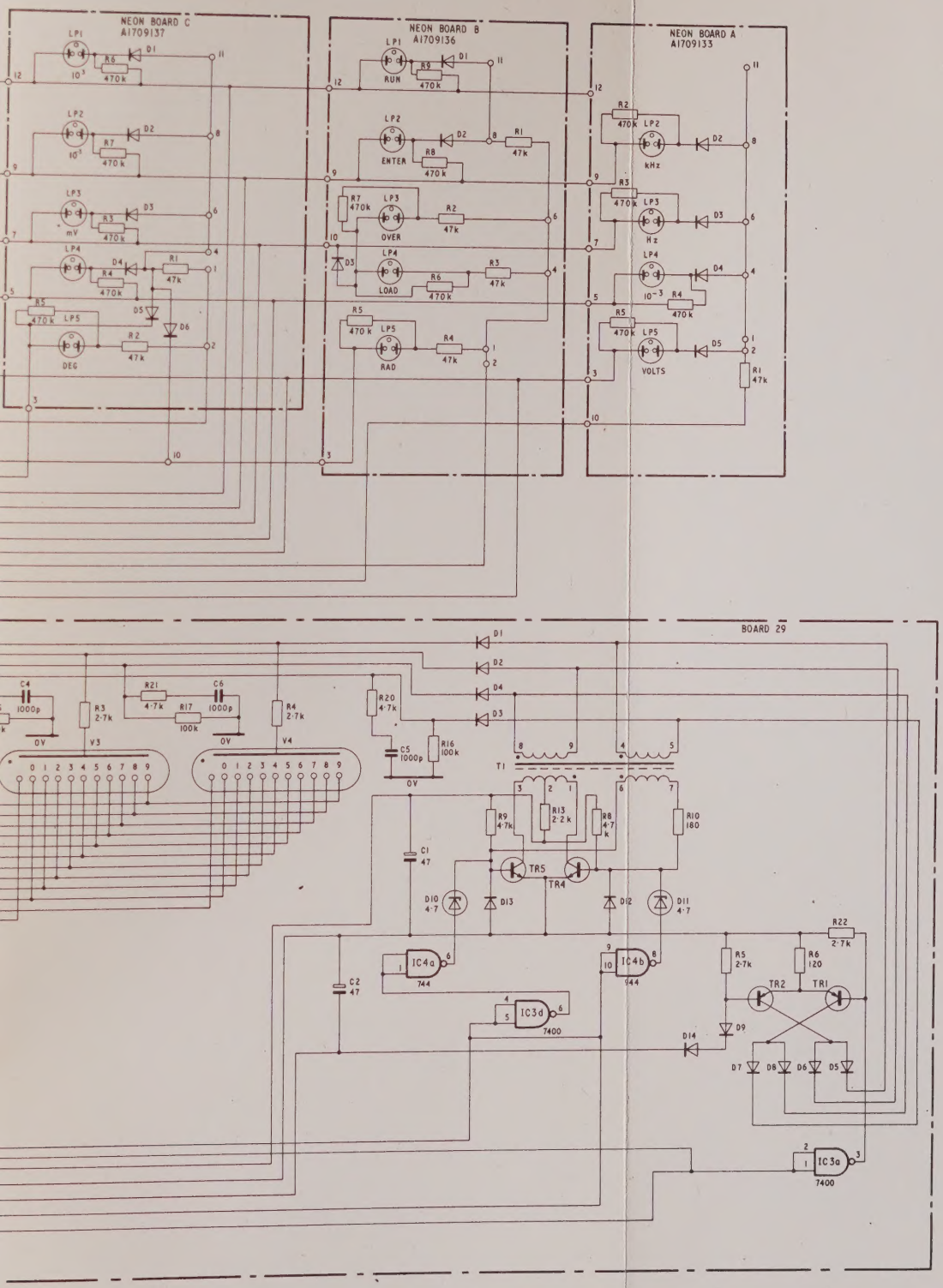


SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2


SKP
TO CCT 75
R5 2.7K
R6 2.7K
R7 2.7K
R8 2.7K
V5
V6
V7
V8
7414
IC9
74 41
IC10
7475
IC11
7475
PLP
TO CCT 75
TR7
TR8
TR6
ALL 40327
TR1
TR2
TR3
TR4
TR5
+5V
C2 ·047
C3 33
C1 ·047
R9 680
R10 680
R11 680
R18 1·2K
R12 680
R13 680
R14 680
R15 680
R16 680
PLM
INVALID 25 1



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTIO


NEON BOARD C
A1709137
NEON BOARD B
A1709136
NEON BOARD A
A1709133
RUN
ENTER
OVER
LOAD
RAD
DEG
kHz
Hz
VOLTS
BOARD 29
TR1
TR2
TR4
TR5
T1
IC4a
IC4b
IC3d
IC3a
7400